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VOL. 10 No. 91 JANUARY 1968

Mullard Technical Communications

VOLUME 10 NUMBER 91

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All articles in *Mullard Technical Communications* are indexed in *British Technology Index*. Abstracts appear in *Current Papers in Physics, Electrotechnology, and Control.*

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Editor: F. A. Sowan
Assistant Editors: E. G. Evans A. Perry

Published by
Central Technical Services
Mullard Limited, Mullard House, Torrington Place, London, W.C.1
Telephone: 01-580 6633 Telex: 264341

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Made and Printed in England by
WIGHTMAN AND COMPANY LIMITED, 1/3 BRIXTON ROAD, LONDON, S.W.9

V.H.F. Transistor Transmitters for A.M. and F.M. Operating Directly from Vehicle Batteries

L. M. Cash
Mullard Central Application Laboratory

This article provides and discusses circuits for battery operated a.m. and f.m. transmitters in the 80MHz and 170MHz bands, with outputs from 7W to 30W for mobile and base stations. The transistors used are the silicon power transistors BLY33, BLY35 and BLY36. The BLY33 and BLY35 are particularly suitable for a.m. operation from a nominal 13·8V supply, or for f.m. from a stabilised 28V supply. The BLY34 and BLY36, with their higher gains, are suitable for f.m. operation from a nominal 13·8V supply.

INTRODUCTION

The Mullard BLY33, BLY34, BLY35 and BLY36 silicon transistors have been developed for class C operation throughout the v.h.f. bands in mobile and base station transmitters. The BLY33 and BLY35 are particularly suitable for a.m. and the BLY34 and BLY36 are particularly suitable for f.m.

The BLY35, in the TO-60 encapsulation, may be used for carrier powers of at least 7W with up to 100% amplitude modulation. The BLY36 has at least 10W f.m. capability.

The BLY33 has been developed to drive the BLY35. It is in the TO-39 encapsulation and also has ratings allowing 100% amplitude modulation at a carrier power of about 2·5W. Similarly, the BLY34 may be used to drive the BLY36 in the 170MHz band.

Each of these transistors operates in circuits with a nominal 12V battery supply and may therefore be used in mobile transmitter-receivers without d.c. converters for supplying h.t.

The circuits shown in Table 1 have been designed to illustrate the variety of transmitter applications satisfied by the BLY33, BLY35 and BLY36. The circuits are described fully on subsequent pages.

V.H.F. mobile transmitter equipment designed to operate with silicon power transistors directly from a vehicle battery, without a d.c. converter, gives better reliability and lower power consumption. From a long term point of view the cost is likely to be less.

This article is intended as a design guide for a.m. and f.m. transmitter circuits operating in the 68 to 87MHz ('low') band and 156 to 174MHz ('high') band operating directly from battery supplies. In general, equipment operating directly from a nominal 12V battery must operate satisfactorily over a range of 11V (during emergency conditions on a run-down battery) to 16·5V (under extreme low temperature on-charge conditions). The circuits described below are designed for a nominal supply voltage of 13·8V which is midway between these extremes, and represents a typical on-charge voltage.

The power transistors BLY33, BLY34, BLY35 and BLY36 are designed to withstand an extreme battery voltage of 20% above nominal (up to 16·5V) without catastrophic failure, and also to permit simultaneous mismatch or mistuning of the load. Normally, severe mismatch conditions would occur for short periods during initial tuning, but if they were permitted for a continuous period of any great length, during fault conditions for example, some deterioration of transistor performance or life might occur, if the dissipation ratings were exceeded.

TABLE 1

Circuits Described in this Article

Transistors	Class of Modulation	Frequency Band (MHz)	Supply Voltage (V)	Carrier Power (Minimum) (W)	Fig. No.
BLY33, BLY35	a.m.	80	13·8 (nom.)	7	8
BLY33, BLY35	a.m.	170	13·8 (nom.)	7	1 and 4
BLY33, BLY35	a.m.	170	13·8 (nom.)	11	1 and 7
BLY33, BLY35	a.m.	170	13·8 (nom.)	15	1 and 7
BSX61, BLY36	f.m.	80	13·8 (nom.)	15	13
BLY33, BLY35	f.m.	170	28 (stab.)	25 to 30	9 and 11

A.M. Transmitters

A.M. HIGH-BAND TRANSMITTERS

These circuits are designed for amplitude modulation depths of up to 100% and total harmonic distortion of the carrier envelope of less than 5% at a modulation depth of 80%.

A common low-power unmodulated front-end can be used for the 7, 11 and 15W transmitter output sections. This low-power front-end (See Fig. 1) can deliver between 350mW and 400mW at the carrier frequency. The photographs in Fig. 2 and Fig. 3 are of a laboratory version of the circuit of Fig. 1.

Land mobile transmitters generally require a certain frequency stability over a stated ambient temperature range and also require strict limitations on the spurious radiated power beyond the permitted bandwidth. In the United Kingdom, the G.P.O. specification (Ref. 1) for transmitters in 80MHz and 170MHz bands, with 25kHz operation, requires suppression (of spurious radiations) below 2·5μW at all frequencies separated from the carrier by more than 50kHz. In addition the equipment must be maintained at ambient temperatures of firstly −10°C and then +40°C for at least one hour and then (in each case) switched 'on' in the standby condition for at least 5 mins. The drift of the carrier must be less than ±3·0kHz for mobile and ±1·5kHz for fixed or base station, relative to the nominal carrier frequency.

The spurious radiations are affected by the number of tuned circuits, in the transmitter line up, at carrier frequency and also by the linearity of modulation.

Low-power Front-end for High-band A.M. Transmitters

It is technically feasible to generate r.f. power at the carrier frequency in the 156 to 174MHz band from a crystal oscillator but high-overtone crystals are more expensive and the tolerances are not so close as with lower overtone crystals. A third-overtone crystal at one third of the carrier frequency was therefore used, followed by a frequency trebler stage. A single stage crystal oscillator-multiplier was rejected because it was found that silicon transistors and crystals of high activity sometimes combined to produce unwanted responses when the oscillator harmonic output circuit was tuned near to its resonance.

It was considered desirable to have three stages tuned to the carrier frequency in the complete transmitter: the low-power front-end itself has two stages at carrier frequency.

The circuit of the front-end (Fig. 1) was built in the laboratory on a printed wiring board. The first stage is a BF115 (TO-72) common base crystal-controlled oscillator at 56·93MHz using a third-overtone all-glass crystal operating in series mode, and tapped about one turn from the earthy side of an eight-turn output coil.

The relatively low input and output capacitances of the BF115 reduce spread of oscillator frequencies between transistor samples, and also reduce the probability of spurious responses caused by the varactor effect of the collector-base diode when the output circuit is brought on tune.

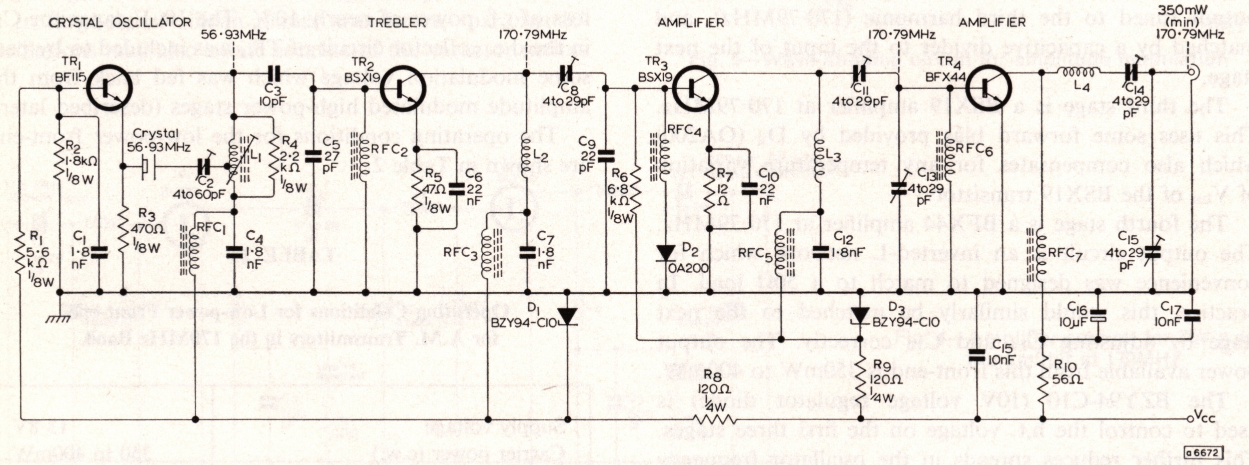

Fig. 1—Front-end for a.m. transmitters at 170MHz

CRYSTAL	Mullard all-glass quartz crystal QX3000, 56·93MHz (third-overtone)	L_4	4 turns of 18 s.w.g. en.cu.; diameter 8mm, length 8 mm
L_1	8 turns of 26 s.w.g. en.cu.; wound on 7mm former; tapped 1 turn from 'earthy' end; slug-tuned	$RFC_{1, 3, 5, 7}$	2½ turns on ferrite bead FX1898 (Mullard)
$L_{2, 3}$	2 turns of 18 s.w.g. en.cu.; diameter 6·4mm, length 5mm	$RFC_{2, 4, 6}$	2 turns of 26 s.w.g. en. cu. wound on ferrite bead FX1115 (Mullard)

To reduce frequency-pulling from the second stage, the output circuit of the oscillator is loaded with a 2·2kΩ resistor and is matched to the input of the next stage by a capacitive divider across the output circuit. A trimmer capacitor should be used, in series with the crystal, to pull the oscillator exactly on to the correct frequency. In this circuit, the oscillator frequency could be pulled over a range of 3kHz by changing the series capacitor from 10pF to 100pF. The oscillator stability against temperature was measured and found to be ±2 to ±3 parts in 10^6 over the range −20°C to +60°C. The Mullard class-0 all-glass quartz crystal units QX3000 (miniature third-overtone 10 to 61MHz), QX3001 and QX3002 (subminiature third-overtone 20 to 61MHz) guarantee a frequency tolerance of less than 20 parts per million and a frequency drift of less than ±10 parts per million over a temperature range of −20°C to +70°C (Ref. 2).

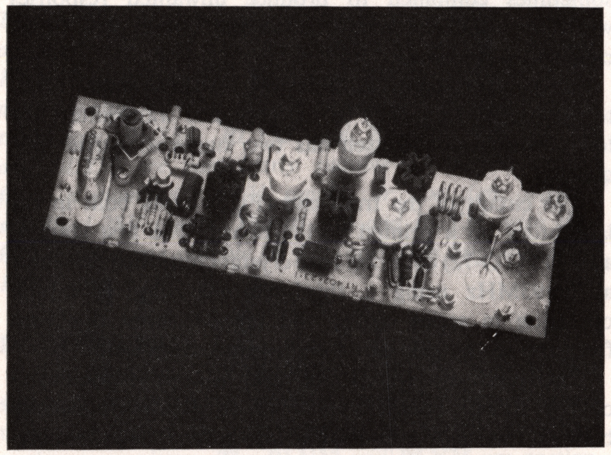

Fig. 2—View of top-side of front-end in Fig. 1

The second stage is a BSX19 frequency trebler, with the output tuned to the third harmonic (170·79MHz), and matched by a capacitive divider to the input of the next stage.

The third stage is a BSX19 amplifier at 170·79MHz. This uses some forward bias provided by D_2 (OA200) which also compensates for any temperature variation of V_{be} of the BSX19 transistor.

The fourth stage is a BFX44 amplifier at 170·79MHz. The output circuit is an inverted-L network which for convenience was designed to match to a 50Ω load. In practice, this would similarly be matched to the next stage by adjusting C_{14} and C_{15} correctly. The output power available from this front-end is 350mW to 400mW.

The BZY94-C10 (10V voltage regulator diode) is used to control the h.t. voltage on the first three stages. This further reduces spreads in the oscillator frequency and in output power of the front-end, despite the variations to be expected in the battery voltage.

Depending on particular requirements, it may be possible to make either of the trimmer capacitors (C_{11} or C_{13} in Fig. 1) a fixed capacitor, and perhaps either C_{14} or C_{15} could also be fixed: this would simplify production. The circuit can be tuned over the 156 to 174MHz band, and the crystal-oscillator frequency would therefore be between 52·0 and 58·0MHz.

Practical Printed Circuit Board for Low-power Front-end

The photograph in Fig. 2 shows that the top-side of the printed circuit board for the front-end has an earthy plate on which the components are mounted through small holes. The under-side of this board, shown in Fig. 3, has an earth-strip perimeter connected to the top earth plate at twelve approximately equidistant points along the edge by soldered dip links. The interconnections on the board are made as broad as possible, and the actual thickness of copper plate was 0·0014in on Fibreglass reinforced plastic board. It must be emphasised that the final BFX44 transistor (TR_4) should have an extremely short emitter lead: this lead should be less than 2mm and should be soldered to the top earth plate using, if necessary, a small post. When the soldered connection was only made by connecting the emitter to the under-side 'earth' then the emitter lead length was 2mm longer because of the printed board thickness; this resulted in a loss of r.f. power of nearly 10%. The 10µF capacitor C_{16} in the d.c. collector circuit of TR_4 was included to by-pass some modulation voltage which was fed back from the amplitude modulated high-power stages (described later).

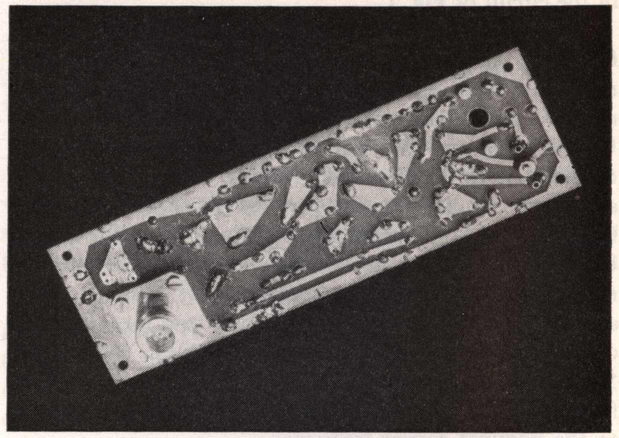

Fig. 3—View of the under-side of front-end in Fig. 1

The operating conditions for the low-power front-end are shown in Table 2.

TABLE 2

Operating Conditions for Low-power Front-end for A.M. Transmitters in the 170MHz Band.

Supply voltage			13·8V
Carrier power (c.w.)			350 to 400mW
Total current			118mA
Oscillator frequency			56·93MHz
Output frequency			170·79MHz
Transistor Operating Conditions		V_{ce}	I_c
Oscillator	(BF115)	7·9V	4·4mA
Trebler	(BSX19)	9·4V	13mA
1st Amplifier	(BSX19)	9·8V	17mA
2nd Amplifier	(BFX44)	10·7V	55mA

High-power Amplifier Stages for 7W A.M. in the High-band

The front-end described above constitutes the first four stages of the 7W a.m. transmitter for the high-band. The circuit of the final two high-power stages is shown in Fig. 4. These stages consist of a BLY33 (TO-39) driver and a final BLY35 (TO-60) power amplifier stage. The r.f. input power required by the BLY33 driver is about 350mW, and modulation is applied to both the BLY33 driver and BLY35 power amplifier stages. The output circuit of the low-power driver stages (Fig. 1) and the input circuit of the high-power stages (Fig. 4) are shown with a matching network for a 50Ω system: this was originally made for the convenience of laboratory measurements. In practice, the output circuit from the low-power front-end would become the input circuit to the BLY33 in Fig. 4. Therefore, in practice, C_1, C_2 and L_1 of Fig. 4 can be omitted.

The output from the BLY33 driver transistor is taken via the matching network C_5, C_6, L_3 (in Fig. 4) to the final BLY35 power amplifier stage which uses an inverted-L output circuit to match to the 50Ω dummy load or aerial.

To obtain reasonable modulation performance it is necessary to apply collector modulation to both the BLY33 driver and the BLY35 power amplifier stages. The full modulation is applied to the BLY35, but a modulation wave-shaping circuit, shown in Fig. 4 and redrawn in Fig. 5, is used to clip the trough of the audio waveform applied to the BLY33 driver. The shaping circuit uses two OA202 diodes arranged across the secondary of the modulation transformer. This circuit improves the modulation waveform obtained from the final power amplifier stage.

Parasitic oscillations can occur in amplifier circuits and methods to suppress these are well known (Ref. 3). Parasitics usually occur near the signal frequency and may be generated even when no signal is present.

In large-signal silicon planar transistors, 'parametric' oscillations may also occur because of the varactor action (that is, voltage dependent capacitance) of the collector-base diode and perhaps the emitter-base diode of the transistor. The frequency of these 'parametric' oscillations is below the signal frequency and occurs when, for example, two tuned circuits can be found such that the sum or difference of their resonance frequencies equals the signal frequency. In transistor power amplifiers, one tuned circuit is in the collector choke together with the collector and output capacitance of the transistor, and the other tuned circuit is the output circuit itself. In the initial development of the 170MHz 7W a.m. transmitter, 'parametric' oscillations occurred at about 4MHz, and in general, parametric oscillations occur at frequencies between 1 and 10MHz.

Parametric oscillation is far more difficult to suppress in amplitude modulated amplifiers than in frequency modulated amplifiers, because in the former case the collector voltage swing is much greater.

The suppression of the parametric oscillation which occurred in the original amplifier design required two modifications to the circuit (Fig. 4). First, a 'parametric trap' C_8 R_4 and L_2 C_4 R_1 was placed in the collector circuits. The coils L_2 and L_4, replacing the r.f. resonant chokes at 170MHz, were made as small as possible; whilst presenting negligible damping to the carrier frequency they act as short-circuits to the parametric frequency which is suppressed through the 10nF and 10Ω series

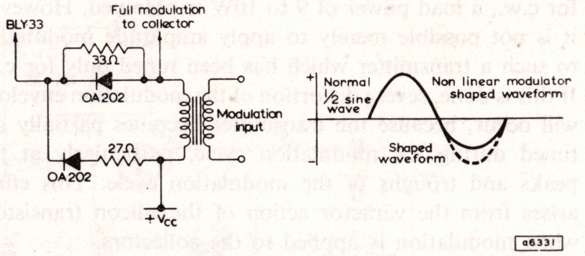

Fig. 5—Wave-shaping circuit for amplitude modulation

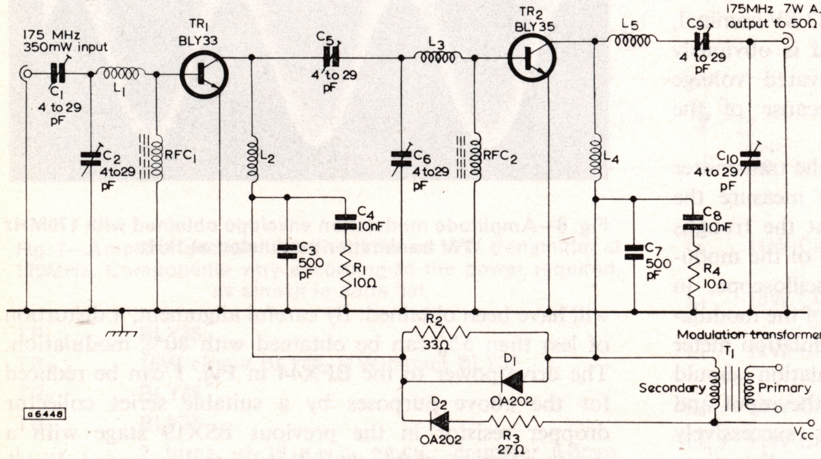

Fig. 4—Amplifier section for 7W a.m. transmitter at 170MHz

$L_{1,\,3}$	3 turns of 18 s.w.g. en.cu.; diameter 6·4mm, length 5mm
$L_{2,\,4}$	5 turns of 18 s.w.g. en.cu.; diameter 6·4mm, length 10mm
L_5	3 turns of 16 s.w.g. en.cu.; diameter 10mm, length 10mm
$RFC_{1,\,2}$	2 turns of 26 s.w.g. en.cu.; wound on ferrite bead FX1115 (Mullard)

combination. By itself this was generally satisfactory when no modulation was applied and it was possible to detune both input and output circuits (C_5, C_6, C_9, C_{10}) without producing parametric oscillation. However, when a high amplitude modulation was applied, it was found possible to produce a low level of parametric oscillation usually with a unique combination of C_5, C_6, C_9, C_{10}, sometimes not very far from the normal tuning position. (It was convenient to observe the parametric oscillation by putting an oscilloscope on its 5mV/cm vertical range across the 10Ω resistor in the parametric trap circuit). Finally the parametric oscillations were completely suppressed, even with 100% modulation, by using a smaller ferrite bead base choke of two turns on the FX1115 ferrite bead. In general, this parametric suppression should be used for all stages of a transmitter to which amplitude modulation is applied. In f.m. transmitters, parametric suppression is generally required only in the high-power stages.

It must be emphasised that the emitter lead of the BLY33 (which is operating at a relatively high-power level) must be short, that is, not greater than 1·6mm. A lead length of 6·3mm for example would seriously reduce the output power, perhaps by 10% or 15%, and also the modulation performance.

Alignment of 7W Transmitter for A.M. Operation

When the above 7W a.m. transmitter is correctly tuned for c.w., a load power of 9 to 10W is obtained. However, it is not possible merely to apply amplitude modulation to such a transmitter which has been tuned only for c.w. If this is done, severe distortion of the modulation envelope will occur, because the transmitter becomes partially detuned during the modulation cycle, particularly at the peaks and troughs of the modulation cycle. This effect arises from the varactor action of the silicon transistors when modulation is applied to the collectors.

Theoretically, for acceptable modulation linearity, the modulated stages should be tuned at a collector voltage equivalent to the voltage at the peak of the modulation cycle where the power requirement from the device is greatest: at 80% modulation and at $V_c = 13{\cdot}8$V nominal, this voltage would be 24·8V. This method is obviously impracticable because tuning at this elevated voltage could rapidly destroy the transistors because of the high collector dissipation.

One method which can be used to align the transmitter for a.m. requires a modulation meter to measure the modulation percentage at the peaks and at the troughs of the carrier envelope. (A visual indication of the modulation waveform was obtained on an oscilloscope, in the laboratory, from the 750kHz i.f. output of the modulation meter, while the a.f. output of the modulation meter was fed to a wave analyser.) The modulation should first be set at a low level, say 25%, and the input and output circuits of the modulated stages successively tuned and retuned for minimum modulation distortion. In the initial steps of this process, the visual assessment from the oscilloscope is sufficient.

The modulation depth should be gradually increased, in one or two steps, to 80% and at each step the successive tuning and retuning of the circuit is repeated until the distortion is reduced to a minimum. The relative modulation peak-to-trough ratio should be unity but, in practice, at the high percentages of modulation, the peak modulation is usually slightly less than the trough modulation, indicating some distortion. If the relative peak-to-trough ratio is not worse than 78:82 (for average m = 80%) this usually indicates a reasonable modulation envelope. This method requires relatively complicated equipment but, although somewhat laborious, does give good results.

Another method which can be used requires relatively simple equipment. The tuning procedure is also simpler and a.m. is not required during the alignment. The method described is empirical and has been used for the 7W a.m. transmitter (Fig. 4), but the principle applies to a.m. alignment in general.

With no modulation on the two normally modulated stages, the r.f. power drive from the low-power drive unit is reduced so that when the last three transmitter stages are tuned for maximum output, a c.w. load power of only 5·5 to 5·8W is obtained, with the supply voltage at 13·8V. (Normally, with full drive from the low-power unit, the load power is 9W to 10W). When the drive from the low-power front-end is gradually returned to its normal value, the final load power, with the tuning left as previously arranged for 5·5 to 5·8W, is approximately 7W to 8W depending upon transistor spreads. If modulation is then applied, reasonably low modulation distortion will have been obtained. By careful alignment, a distortion of less than 5% can be obtained with 80% modulation. The drive power to the BFX44 in Fig. 1 can be reduced for the above purposes by a suitable series collector dropper resistor in the previous BSX19 stage with a shorting link to enable the full drive to be retuned. Fig. 6 shows the a.m. waveform obtained from the 170MHz 7W transmitter when correctly aligned.

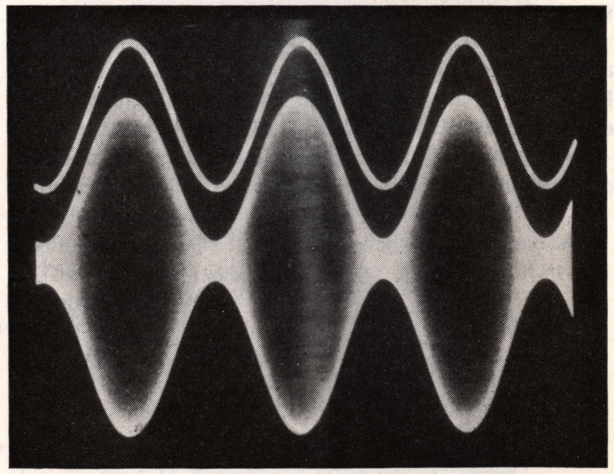

Fig. 6—Amplitude modulation envelope obtained with 170MHz 7W transmitter modulated at 1kHz

The operating conditions for the 7W transmitter described are shown in Table 3. Altogether, four such transmitters were constructed in the laboratory, three with normal metal chassis construction, and the results were entirely repeatable.

High-power Stages For 11W A.M. High-band Transmitter

The front-end shown in Fig. 1 may also be used for the 11W a.m. transmitter. The final three modulated stages for 11W, shown in Fig. 7, require an r.f. input of only 70 to 80mW. The front-end can deliver 350 to 400mW and it is necessary to reduce the output of the front-end by a factor of 5 (that is, 7dB). This may be done by using d.c. collector resistors, or by increasing the emitter resistors of some stages, or by inserting a simple π-network between the front-end and modulated power stages to attenuate the input to these power stages. The final three modulated amplifier stages of the 11W a.m. transmitter are a BLY33 pre-driver, a BLY33 driver and two parallel BLY35 power amplifier stages. In the final BLY35 parallel transistors, the collectors are connected together and the emitters are connected together, but it is necessary to take the input from the BLY33 driver stage to the base of each BLY35 through a separately tuned matching network. Tuning these independently for maximum output power tends to equalise the collector currents of these transistors. The modulation voltage is taken directly to the collectors of the driver and output transistors, but the modulation is taken via a wave-shaping circuit (Fig. 5) to the collector of the BLY33 pre-driver transistor. Parametric oscillation traps are included in the collector

TABLE 3

Operating Conditions for 7W High-band Amplifier Stages

Supply voltage		13·8V	
Carrier output power (minimum)		7W	
Drive power (c.w.)		(approx) 350mW	
Modulation		up to 100%	
Modulation linearity		<5% distortion at 80% modulation	
Total current			
(excluding low-power front-end)		(approx) 880mA	
(including low-power front-end)		(approx) 1A	
Carrier frequency		170·79MHz	
Transistor Operating Conditions		V_{ce}*	I_c
Driver	(BLY33)	12·8V	220mA
Output	(BLY35)	13·6V	660mA

*An h.t. voltage drop of 0·2V occurs in the resistance of the modulation transformer winding and 0·8V in the driver modulation wave-shaping circuit.

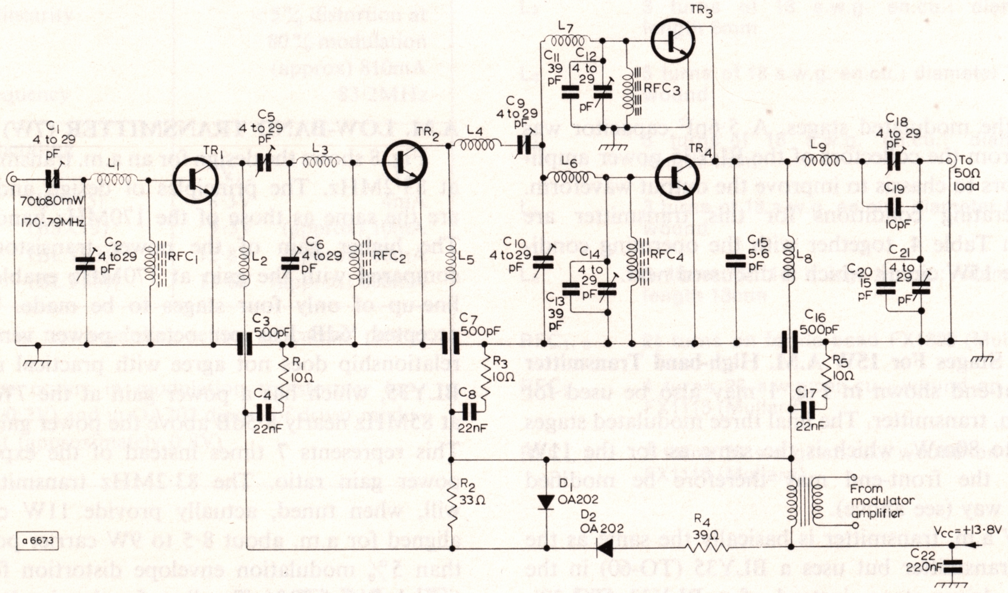

Fig. 7—Amplifier section for either 11W or 15W transmitter at 170MHz. Components vary according to the power required, as shown in parts list

TR_1		BLY33
TR_2		15W circuit BLY35, 11W circuit BLY33
TR_3		BLY35
TR_4		BLY35
L_1		2 turns of 18 s.w.g. en.cu.; diameter 6·3mm, length 10mm
$L_{2, 5, 8}$		5 turns of 18 s.w.g. en.cu.; diameter 6·3mm, length 9mm
L_3	15W Circuit	2 turns of 18 s.w.g. en.cu.; diameter 6·3mm, length 5mm
L_3	11W Circuit	3 turns of 18 s.w.g. en.cu.; diameter 6·3mm, length 6mm
L_4	15W Circuit	2 turns of 16 s.w.g. en.cu.; diameter 6·3mm, length 5mm
L_4	11W Circuit	3 turns of 18 s.w.g. en.cu.; diameter 6·3mm, length 6mm
$L_{6, 7}$	15W Circuit	1 turn of 16 s.w.g. en.cu.; diameter 6·3mm
$L_{6, 7}$	11W Circuit	3 turns of 18 s.w.g. en.cu.; diameter 6·3mm, length 5mm
L_9		2 turns of 14 s.w.g. en.cu.; diameter 10mm, length 6mm
$RFC_{1, 2, 3, 4}$		2 turns of 26 s.w.g. en.cu.; wound on ferrite bead FX1115 (Mullard)

TABLE 4

Operating Conditions for High-band 11W and 15W Transmitters

		11W Circuit	15W Circuit
Supply voltage		13·8V	13·8V
Carrier power (c.w.)		11W	15W
Modulation		100%	100%
Modulation linearity		<5% distortion at 80% modulation	<5% distortion at 80% modulation
Drive power requirement		(approx) 70mW	(approx) 70mW
Total current			
(excluding low-power front-end)		(approx) 1·2A	(approx) 1·6A
(including low-power front-end)		(approx) 1·3A	(approx) 1·7A
Collector voltage*			
Pre-driver	(BLY33)	12·8V	12·8V
Driver	(BLY33)	13·6V	
	(BLY35)		13·6V
Output	(2×BLY35)	13·6V	13·6V
Collector current			
Pre-driver	(BLY33)	(approx) 25mA	(approx) 30mA
Driver	(BLY33)	(approx) 170mA	
	(BLY35)		(approx) 200mA
Output	(2×BLY35)	(approx total) 1·0A	(approx total) 1·35A

*Voltage drop occurs in the modulation transformer (approximately 0·2V) and in OA202 diodes of pre-driver modulation circuits (approximately 0·8V).

circuits of the modulated stages. A 5·6pF capacitor was connected from the collectors of the BLY35 power amplifier transistors to chassis to improve the output waveform.

The operating conditions for this transmitter are displayed in Table 4, together with the operating conditions for the 15W circuit which is discussed next.

High-power Stages For 15W A.M. High-band Transmitter

The front-end shown in Fig. 1 may also be used for the 15W a.m. transmitter. The final three modulated stages require 70 to 80mW, which is the same as for the 11W transmitter; the front-end may therefore be modified in the same way (see above).

The 15W a.m. transmitter is basically the same as the 11W a.m. transmitter but uses a BLY35 (TO-60) in the penultimate driver stage, instead of a BLY33 (TO-39). The circuit (Fig. 7) is the same as for the 11W transmitter with some component changes.

The operating conditions for the 15W transmitter are shown in Table 4.

Alignment of 11W and 15W A.M. Transmitters

The principle of the procedure used to align the 11W and 15W transmitters is the same as that for the 7W transmitter. The c.w. setting under the necessary reduced drive conditions should be 8·8 to 9·2W for the 11W transmitter and 12·0 to 12·5W for the 15W transmitter.

A.M. LOW-BAND TRANSMITTER (7W)

Fig. 8 shows the design for an a.m. transmitter operating at 83·2MHz. The principles of design and construction are the same as those of the 170MHz band transmitters. The higher gain of the power transistors at 80MHz compared with the gain at 170MHz enables a complete line-up of only four stages to be made. The generally accepted '6dB loss per octave' power versus frequency relationship does not agree with practical results for the BLY35, which has a power gain at the 7W output level at 85MHz nearly 8·5dB above the power gain at 170MHz. This represents 7 times instead of the expected 4 times power gain ratio. The 83·2MHz transmitter in Fig. 8 will, when tuned, actually provide 11W c.w., or when aligned for a.m. about 8·5 to 9W carrier power with less than 5% modulation envelope distortion for a modulation depth of 80%. To allow for the simultaneous occurrence of high battery voltage operation and 100% modulation, and mismatch or mistuning of the power stage to the aerial load, it is not permissible to operate the BLY35 above the 7 to 8W a.m. rating. (This rating is a minimum carrier power rating for 7W up to 100% modulation and may spread up to a maximum of 8W because of transistor spreads). It is therefore desirable to put a small resistor in the common d.c. collector leads of the last two stages to drop the supply voltage to give 7 to 8W carrier power.

The operating conditions for the 7W a.m. low-band transmitter are given in Table 5.

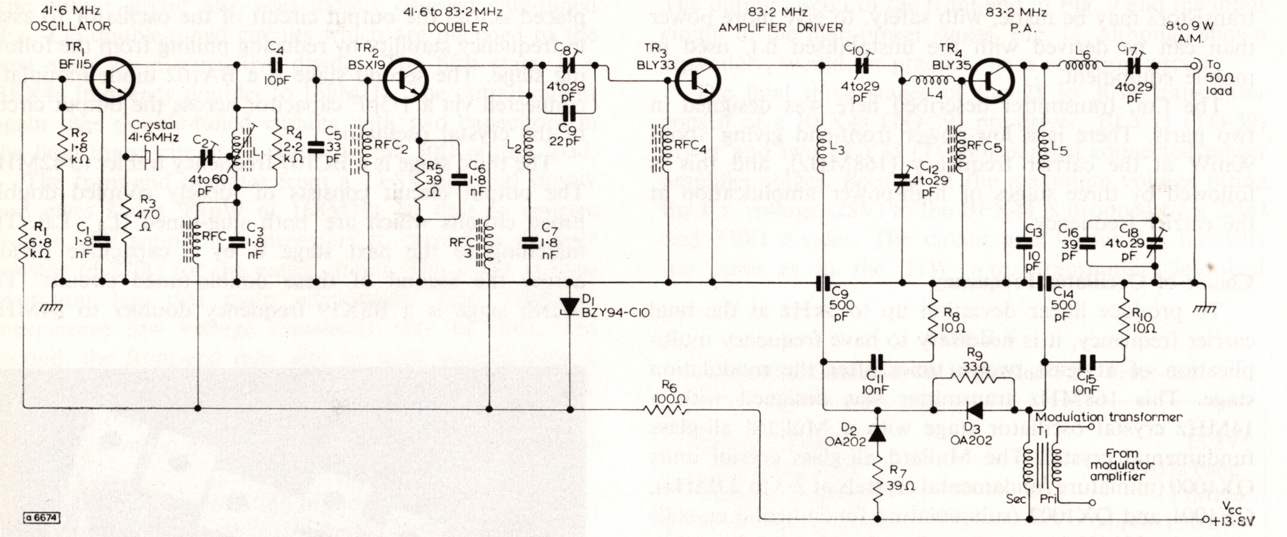

Fig. 8—Complete transmitter for 7W a.m. transmitter at 83·2MHz

TABLE 5

Operating Conditions for 7W Low-band Transmitter

Supply voltage			13·8V
Carrier power*			minimum 7W
Modulation			up to 100%
Modulation linearity			<5% distortion at 80% modulation
Total current			(approx) 810mA
Operating frequency			83·2MHz
Transistor Operating Conditions		V_{ce}	I_c
Oscillator	(BF115)	8·3V	4mA
Doubler	(BSX19)	9·5V	(approx) 10mA
Driver	(BLY33)†	12·8V	(approx) 80mA
Output	(BLY35)†	13·6V	(approx) 680mA

*See remarks in text regarding setting of carrier power level.

†Voltage drop occurs in modulation transformer (approximately 0·2V) and in OA202 diodes of driver modulation circuit (approximately 0·8V).

CRYSTAL	Mullard all-glass quartz crystal QX3000, 41·6MHz (third-overtone)
L_1	11 turns of 26 s.w.g. en.cu.; close-wound on 7mm former; tapped 1 turn from 'earthy' end; slug-tuned
L_2	3 turns of 18 s.w.g. en.cu.; diameter 8mm, length 6mm
L_3	5 turns of 18 s.w.g. en.cu.; diameter 7mm, close-wound
L_4	3 turns of 18 s.w.g. en.cu.; diameter 8mm, length 4mm
L_5	3 turns of 18 s.w.g. en.cu.; diameter 8mm, close-wound
L_6	5 turns of 14 s.w.g. en.cu.; diameter 10mm, length 13mm
$RFC_{1,\,3}$	2½ turns on ferrite bead FX1898 (Mullard)
RFC_2	4 turns 26 s.w.g. en.cu.; wound on ferrite bead FX1115 (Mullard)
$RFC_{4,\,5}$	2 turns 26 s.w.g. en.cu.; wound on ferrite bead FX1115 (Mullard)

F.M. Transmitters

F.M. HIGH-BAND TRANSMITTER (25 to 30W)

The circuit to be described is intended to provide 25 to 30W for f.m. transmission, operating from a 28V supply and is therefore most suited for use in fixed base stations. Certain general considerations concerning this type of transistor circuit are discussed first.

Many of the general considerations that affect the design of a.m. circuits also apply to the design of f.m. circuits. Some of the difficulties, however, become simplified with f.m. operation. For example, the power transistors can be operated at nearly twice the maximum h.t. voltage in f.m. circuits, compared with the voltage in a.m. circuits, and so the power gain of the transistors is greater. In addition, the avoidance of parametric oscillations is easier in the absence of collector modulation. Some additional problems may, however, be introduced in f.m. transmitters by the higher frequency multiplication factor required between the oscillator and the final carrier frequency. For fixed base stations there is usually no problem in stabilising the h.t. voltage; therefore the power transistors may be made, with safety, to give more power than can be derived with the unstabilised h.t. used in mobile equipment.

The f.m. transmitter described here was designed in two parts. There is a low-power front-end giving about 90mW at the carrier frequency (168MHz), and this is followed by three stages of high-power amplification at the carrier frequency.

Choice of Oscillator Frequency

To produce linear deviation up to 5kHz at the final carrier frequency, it is necessary to have frequency multiplication of at least twelve times after the modulation stage. This 168MHz transmitter was designed with a 14MHz crystal oscillator stage with a Mullard all-glass fundamental crystal. The Mullard all-glass crystal units QX1000 (miniature fundamental crystals at 2·3 to 20MHz), QX1001 and QX1002 (subminiature fundamental crystals at 7·0 to 20MHz) guarantee, for class-0 crystals, a frequency tolerance of ±20 parts per million and a frequency stability of ±10 parts per million over a temperature range of −15°C to +70°C (Ref. 2).

Low-power Front-end for High-band F.M. Transmitter

The circuit diagram of the low-power front-end is shown in Fig. 9 and a view of the laboratory version is shown in Fig. 10. The first stage is a BF115 common-base crystal-controlled oscillator at 14MHz using the all-glass crystal in the series mode. A 2·7kΩ resistor is placed across the output circuit of the oscillator to assist in frequency stability by reducing pulling from the following stage. The second stage is a BA102 diode modulator connected via a 1·5pF capacitor across the output circuit of the crystal oscillator.

The third stage is a BC107 frequency trebler to 42MHz. The output circuit consists of loosely coupled double-tuned circuits which are both slug-tuned (L_3, L_4). The matching to the next stage is by a capacitive divider across the second of these double-tuned circuits. The fourth stage is a BSX19 frequency doubler to 84MHz.

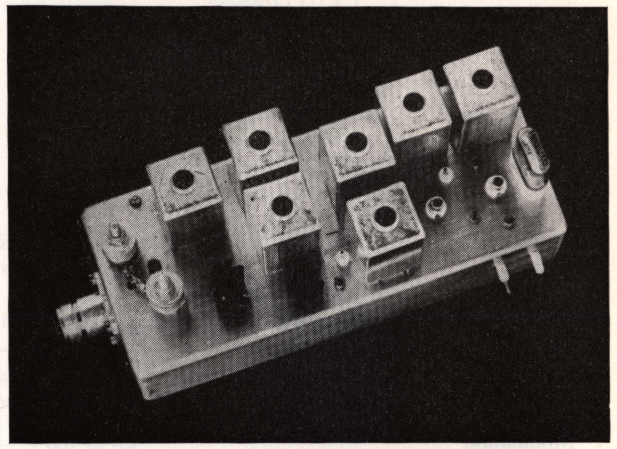

Fig. 10—View of top-side of front-end in Fig. 9

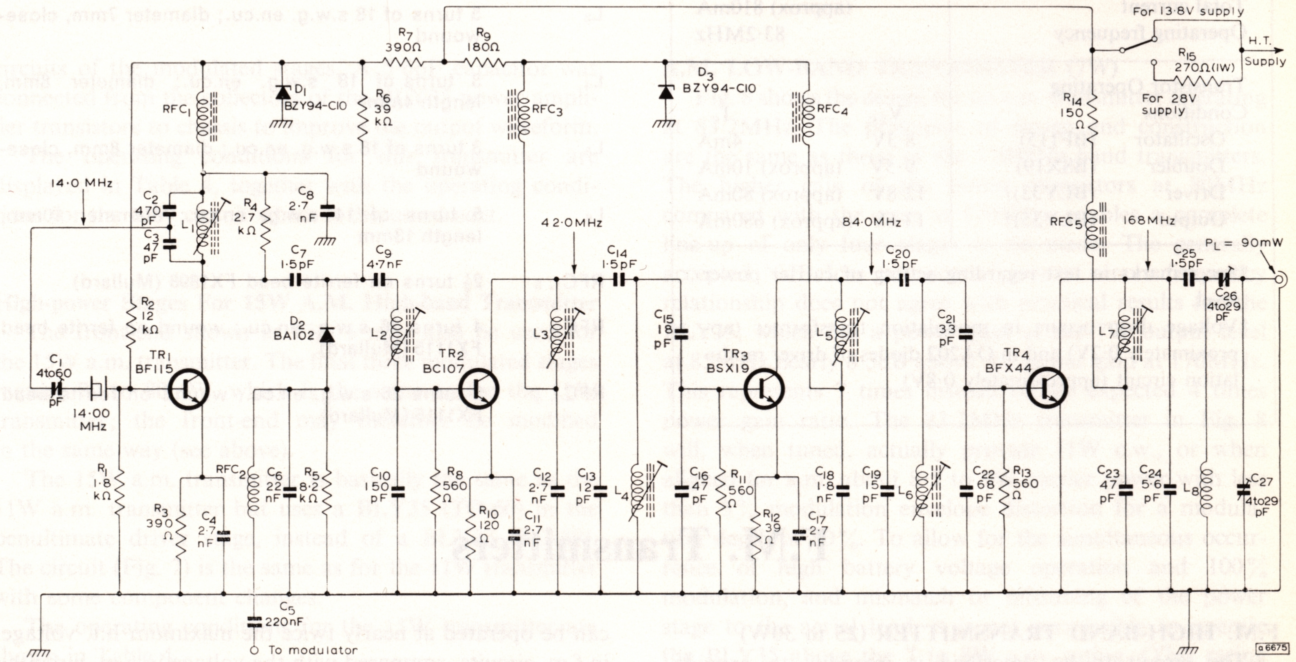
R7 390Ω
R9 180Ω
D1 BZY94-C10
R6 39 kΩ
RFC1
RFC3
D3 BZY94-C10
RFC4
For 13·8V supply
H.T. Supply
R15 270Ω(1W)
For 28V supply
R14 150 Ω
14·0 MHz
C2 470 pF
C3 47 pF
L1
R4 2·7 kΩ
C8 2·7 nF
C7 1·5pF
C9 4·7nF
42·0MHz
C14 1·5pF
84·0MHz
C20 1·5pF
RFC5
168MHz
C25 1·5pF
PL = 90mW
C26 4to29 pF
R2 12 kΩ
D2 BA102
L2
L3
C15 18 pF
L5
C21 33 pF
L7
TR1 BF115
TR2 BC107
TR3 BSX19
TR4 BFX44
C1 4to60 pF
14·00 MHz
R1 1·8 kΩ
R3 390 Ω
C4 2·7 nF
RFC2
C6 22 nF
R5 8·2 kΩ
C10 150 pF
R8 560 Ω
R10 120 Ω
C11 2·7 nF
C12 2·7 nF
C13 12 pF
L4
C16 47 pF
R11 560 Ω
R12 39 Ω
C17 2·7 nF
C18 1·8 nF
C19 15 pF
L6
C22 68 pF
R13 560 Ω
C23 47 pF
C24 5·6 pF
L8
C27 4to29 pF
C5 220nF
To modulator
a6675

Fig. 9—Front-end for 30W 168MHz f.m. transmitter

CRYSTAL	Mullard all-glass quartz crystal QX1000, 14·00MHz (fundamental)
L_1	31 turns of 26 s.w.g. en.cu.; wound on 7mm former, slug-tuned
L_2	34 turns of 26 s.w.g. en.cu.; wound on 7mm former, slug-tuned
$L_{3, 4}$	11 turns of 26 s.w.g. en.cu.; wound on 7mm former, slug-tuned
L_5	5½ turns of 18 s.w.g. en.cu.; wound on 7mm former, slug-tuned
L_6	4 turns of 18 s.w.g. en.cu.; wound on 7mm former, slug-tuned
L_7	2½ turns of 18 s.w.g. en.cu.; wound on 7mm former, slug-tuned
L_8	2½ turns of 18 s.w.g. en.cu.; diameter 6·4mm, length 4mm
$RFC_{1, 3, 4, 5}$	2½ turns on ferrite bead FX1898 (Mullard)
RFC_2	Type 200/511 (Painton)

The output circuit also uses loosely coupled slug-tuned (L_5, L_6) double-tuned circuits which are matched to the next stage by a capacitive divider. The fifth stage is a BFX44 frequency doubler to 168MHz. The output circuit again uses double-tuned circuits with two capacitors in the final tuned circuit to match to the 50Ω output load.

The front-end operates from a 13·8V nominal supply and gives about 90mW at 168MHz, so that to operate from a 28V supply it is necessary to provide a dropper resistor of 270Ω for the entire circuit. The lower voltage operation has two main advantages: first, relatively inexpensive low voltage transistors may be used, and second, the front-end may also be used directly from a 12V battery, if required. The power loss in the 270Ω resistor is negligible for a 25 to 30W transmitter and, in any case, is of no great importance in base station operation.

To obtain 5kHz deviation of the final carrier frequency, 200mV of modulation was required at 1kHz.

The operating conditions of this front-end are displayed in Table 6.

Power Amplifier Stages of 30W F.M. Transmitter

The front-end described above constitutes the first five stages of the 25 to 30W transmitter for the high-band. The circuit of the succeeding power amplifier stages is shown in Fig. 11. The r.f. input requirement for these power stages is approximately 45mW; it is therefore necessary to halve the output power from the front-end. This may be done by inserting collector resistors or increasing the emitter resistor in some of the front-end stages, or by a simple resistive π-network attenuator between the front-end and the power amplifier stages.

The output circuit of the front-end in Fig. 9 and the input circuit of the high-power stages, Fig. 11, although shown separately, would, in practice, be a common circuit.

The final three stages of the 25 to 30W transmitter consist of a BFX44 (TO-39) pre-driver, BLY33 (TO-39) driver and two BLY35 (TO-60) parallel connected power amplifier stages. Because of the maximum voltage rating the h.t. voltage (28V) to the BFX44 is dropped by a 220Ω and 330Ω divider. The circuit and layout are basically the same as in the 11W a.m. transmitter described

TABLE 6

Operating Conditions for High-band F.M. Front-end

Supply voltage*			13·8V*
Carrier frequency			168MHz band
Oscillator frequency			14MHz
Output carrier power			(approx) 90mW
Modulation			Phase modulation
			5kHz deviation at carrier frequency (a.f.=1kHz) for 200mV input to modulator
Total current			48mA
Transistor Operating Conditions		V_{ce}	I_c
Oscillator	(BF115)	9·0V	2·6mA
Trebler	(BC107)	9·6V	3·7mA
1st Doubler	(BSX19)	9·8V	6mA
2nd Doubler	(BFX44)	11·2V	17·5mA

*When this front-end is used with the 25 to 30W amplifier stages described in this article, a 270Ω series dropper resistor should be used with the 28V supply line.

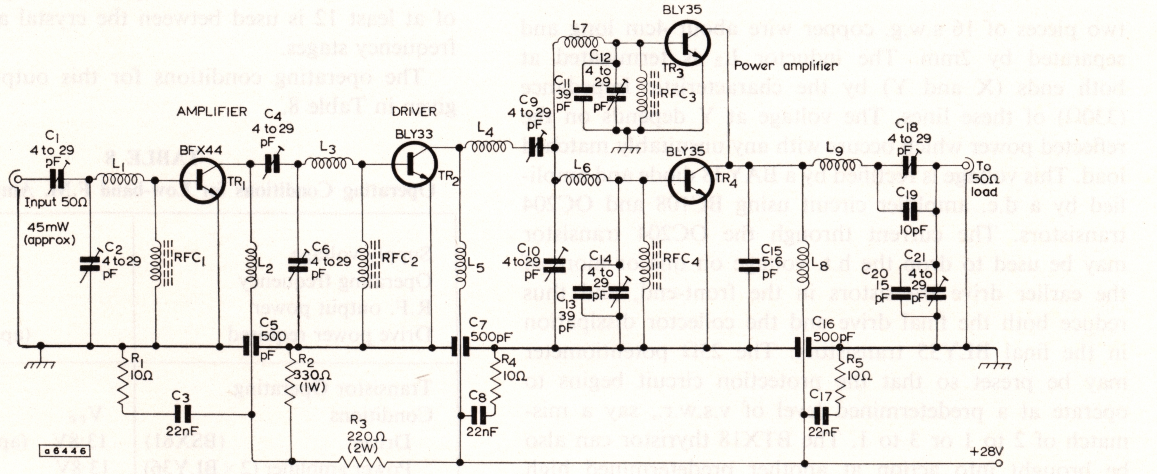
AMPLIFIER
DRIVER
BLY35
Power amplifier
C1 4 to 29 pF
Input 50Ω
45mW (approx)
L1
BFX44
TR1
C4 4 to 29 pF
L3
BLY33
TR2
L4
C9 4 to 29 pF
L7
C12 4 to 29 pF
C11 39 pF
TR3
RFC3
L6
TR4
L9
C18 4 to 29 pF
To 50Ω load
C19 10pF
C2 4 to29 pF
RFC1
L2
C6 4 to29 pF
RFC2
L5
C10 4to29 pF
C14 4 to 29 pF
C13 39 pF
RFC4
C15 5·6 pF
L8
C20 15 pF
C21 4 to 29 pF
C5 500 pF
C7 500pF
C16 500pF
R1 10Ω
R2 330Ω (1W)
R4 10Ω
R5 10Ω
C3 22nF
C8 22nF
C17 22nF
R3 220Ω (2W)
+28V
a6446

Fig. 11—Amplifier stages for 25 to 30W f.m. power at 168MHz

L_1	3 turns of 18 s.w.g. en.cu.; diameter 6·4mm, length 8mm
$L_{2, 4, 5, 8}$	5 turns of 18 s.w.g. en.cu.; diameter 6·4mm, length 10mm
L_3	3 turns of 18 s.w.g. en.cu.; diameter 6·4mm, length 6mm
$L_{6, 7}$	3 turns of 18 s.w.g. en.cu.; diameter 6·4mm, length 5mm
L_9	2 turns of 14 s.w.g. en.cu.; diameter 9·6mm, length 8mm
$RFC_{1, 2, 3, 4}$	2 turns of 26 s.w.g. en.cu.; wound on ferrite bead FX1115 (Mullard)

earlier. Again it must be emphasised that the emitter leads of the TO-39 encapsulated BFX44 and BLY33 must not be longer than 1·6mm, or there will be some loss of output power.

The 30W rating of the two paralleled BLY35 amplifier is only valid if the 28V supply is stabilised. For an unstabilised supply, this power rating must be reduced so that the final load power does not exceed 30W even at the top limit of the supply voltage. In addition, when a 28V line is used it is desirable to have a protection circuit in case of accidental open-circuit, short circuit or severe mismatch of the aerial or load.

The principle of one protection circuit is shown in Fig. 12. It uses the directional coupler method for detection of the voltage standing-wave ratio. L_1 and L_2 are two pieces of 16 s.w.g. copper wire about 4cm long and separated by 2mm. The inductor L_2 is terminated at both ends (X and Y) by the characteristic impedance (330Ω) of these lines. The voltage at Y depends on the reflected power which occurs with any unsuitably matched load. This voltage is rectified by a BAY38 diode and amplified by a d.c. amplifier circuit using BC108 and OC204 transistors. The current through the OC204 transistor may be used to drop the h.t. voltage on one or more of the earlier drive transistors in the front-end, and thus reduce both the final drive and the collector dissipation in the final BLY35 transistors. The 25Ω potentiometer may be preset so that the protection circuit begins to operate at a predetermined level of v.s.w.r., say a mismatch of 2 to 1 or 3 to 1. The BTX18 thyristor can also be brought into action at another predetermined high level of mismatch, say 6 to 1, by the resistor in series with the gate. When the BTX18 is triggered, the drive and the output power are both completely removed and can only be restored after the fault has been cleared and the h.t. switched 'off' and then 'on' again. The latter would occur with the normal press-to-talk facility.

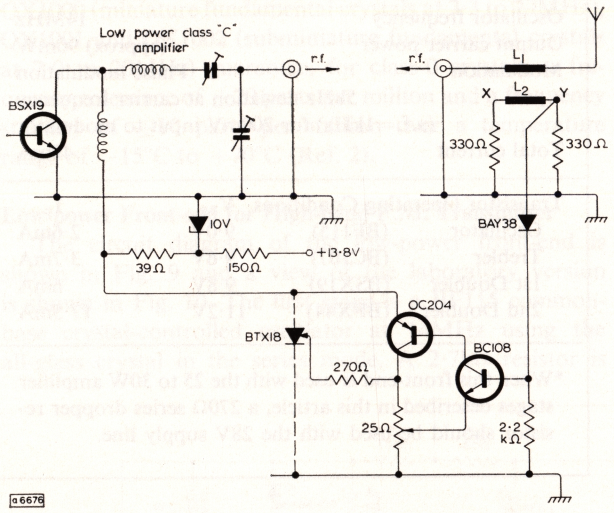

Fig. 12—Protection circuit for 30W 168MHz f.m. transmitter

The operating conditions for the amplifier stages described are given in Table 7.

TABLE 7

Operating Conditions for 25 to 30W High-band Amplifier Stages

Operating voltage*		(stabilised) 28V
Carrier frequency		168MHz band
Output power*		25 to 30W
Required drive power		(approx) 45mW
Total current for 30W		
(excluding low-power front-end)		(approx) 1·62A
(including low-power front-end)		(approx) 1·67A
Transistor Operating Conditions	V_{ce}	I_c
Pre-driver (BFX44)	12·4V	33mA
Driver (BLY33)	28V	196mA
Power amplifier (2×BLY35)	28V	total 1·3A

*Care should be taken during initial tuning and subsequent operation to ensure the load or aerial is correctly matched to the transmitter power stages.

F.M. LOW-BAND TRANSMITTER (15W)

Because of the high gain of the BLY36 at 80MHz, only about 500mW drive power is required by the two parallel-connected BLY36 transistors, to provide 16W load power. It is therefore possible to use an inexpensive high-speed switching type driver transistor, such as the BSX61. The circuit of Fig. 13 shows the last two power stages of a transmitter using a BSX61 driving two parallel-connected BLY36 transistors. The drive requirement of the BSX61 is approximately 40mW at 80MHz. (No front-end for this circuit is described here.)

The principles of circuit design and the layout used here are similar to those for the previously described output stages. For 5kHz deviation at the carrier frequency it is recommended that a frequency multiplication factor of at least 12 is used between the crystal and the carrier frequency stages.

The operating conditions for this output section are given in Table 8.

TABLE 8

Operating Conditions for Low-band F.M. Amplifier Stages

Supply voltage		13·8V
Operating frequency		83·2MHz
R.F. output power		>15W
Drive power required		(approx) 40mW
Transistor Operating Conditions	V_{ce}	I_c
Driver (BSX61)	13·8V	(approx) 60mA
Power amplifier (2×BLY36)	13·8V	1·4A

REFERENCES

1. **'Private Mobile Radio Services'**, G.P.O. Specifications W6345 and W6346.
2. **'Mullard All-glass Quartz Crystal Units'**, TP548, Mullard Ltd., and relevant data sheets (Technical Handbook Vol. 3)
3. Teale, G. S. M., 'Parasitic Oscillations in V.H.F. Power Amplifiers', **Mullard Technical Communications**, Vol. 9, No. 90, Nov. 1967, pp. 279 to 284.

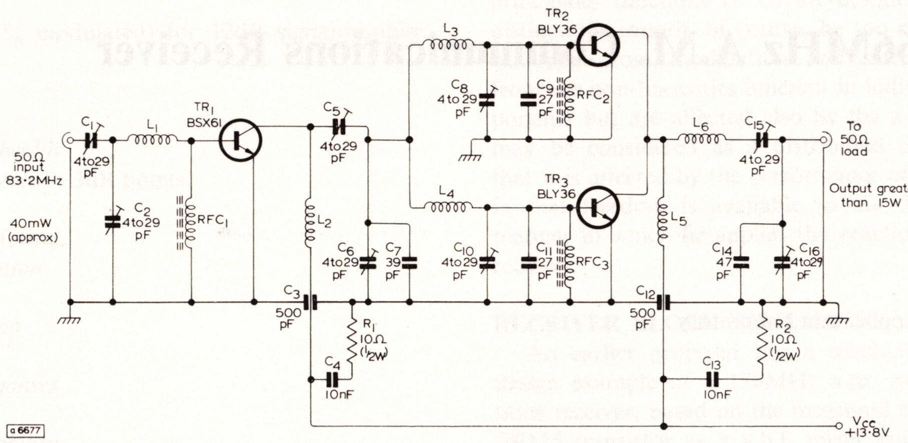

Fig. 13—Power amplifier stages (only) of 15W f.m. transmitter at 80MHz

$L_{1, 2, 5}$	5 turns of 18 s.w.g. en.cu.; diameter 6·4mm, close-wound
$L_{3, 4}$	4 turns of 18 s.w.g. en.cu.; diameter 6·4mm, length 9mm
L_6	5 turns of 16 s.w.g. en.cu.; diameter 10mm, length 11m
$RFC_{1, 2, 3}$	2 turns of 26 s.w.g. en.cu.; wound on ferrite bead FX1115 (Mullard)

Mobile 166MHz A.M. Communications Receiver

D. SINGH
Mullard Central Application Laboratory

A mobile communications receiver has been designed using only silicon planar transistors. The design is suitable for single channel a.m. mobile operation in the 156 to 174MHz band. The prototype receiver passes laboratory tests equivalent to those specified by the G.P.O. for commercial receivers.

Transistors used are BF115, BC108 and BFY52.

The receiver is a single conversion superhet with an intermediate frequency of 10·7MHz. The i.f. section consists of R-C coupled stages. The full selectivity is provided by a block crystal filter at the input of the i.f. section. The audio section uses direct coupled stages and has a non-complementary transformerless output stage providing 1W.

INTRODUCTION

Silicon transistors from the Mullard Practical Planar Range are available in quantity production with good gain and noise performance at 200MHz, making feasible the design of all-silicon mobile communications receivers. In general, planar types are the most suitable for front-end and i.f. stages because of performance and cost, while planar types are suitable also for use in audio stages for their economy and compatibility in polarity with the r.f. stages. Further, silicon v.h.f. power transistors are becoming readily available, making possible the design of all transistor mobile transmitters operating direct from a car battery without a d.c. converter: these v.h.f. transistors are exclusively n-p-n types (Ref. 1).

It was therefore decided to apply these modern silicon transistors in an a.m. mobile communications receiver for the band 156 to 174MHz suitable for 25kHz channel separation. In particular the transistor type BF115 was found to be sufficiently adaptable and economic to be used throughout the r.f. and i.f. stages. The audio transistors chosen were BC108 and BFY52.

RECEIVER SPECIFICATION

The minimum performance required of commercial mobile a.m. receivers operating in the 156 to 174MHz band with 25kHz channel spacing is defined in a G.P.O. Specification (Ref. 2). The main requirements are summarized below; the actual figures of the G.P.O. Specification have been adjusted for a 50Ω input receiver (instead of 75Ω) and voltage levels relate to p.d. at the receiver input instead of open circuit aerial e.m.f.

1) *Receiver Sensitivity*
   The input signal (30% modulation) required to give 10dB signal-to-noise ratio in audio output power should be not greater than 2·0μV.
2) *Selectivity*
   The input level at a frequency ±23·5kHz off-tune required to give the same audio output power as the standard on-tune signal (10dB signal-to-noise ratio) should be not less than 70dB referred to the on-tune signal.
3) *Spurious Responses*
   Spurious signal levels at any frequency required to give the same audio output power as the standard on-tune signal should be not less than 70dB referred to the on-tune signal.
4) *Cross Modulation*
   For an on-tune signal of 0·4mV (unmodulated), the level of interfering signal (30% modulated) at a frequency removed from the on-tune signal by ⩾150kHz should be not less than 13·3mV to give an audio output power −20dB referred to the output, if the on-tune signal were to be 30% modulated, that is, an interfering signal level approximately +30dB referred to the on-tune level.
5) *Intermodulation*
   In a three-generator test the level of either interfering signal should be not less than 50dB referred to the on-tune signal (10dB signal-to-noise ratio) for a reduction of signal-to-noise ratio by 3dB.
6) *Blocking*
   The level of an interfering signal 150kHz or more away from an on-tune signal (10dB signal-to-noise ratio) required to change the audio output power by 3dB should be not less than 13·3mV.
7) *Spurious Radiated Power at the Aerial*
   The level of spurious available power at the aerial terminals should be not greater than 20nW.

Other countries have corresponding minimum performance requirements and it was considered worth examination to discover whether a receiver can, without undue complication, satisfy the major requirements of all relevant specifications simultaneously.

The following is a summary of major performance criteria which could go some way towards satisfying the requirements of all countries regarding mobile v.h.f. a.m. receivers in this frequency band.

1) *Sensitivity*
   $\ngtr$ 0·75μV (30% modulated) for 12dB signal-to-noise ratio.
2) *Selectivity*
   $\nless$ 70dB.
3) *Receiver Bandwidth*
   $\nless$ 12kHz between −3dB points.
4) *Blocking*
   $\nless$ 13mV interfering.
5) *Cross Modulation*
   $\nless$ 30dB.
6) *Intermodulation*
   $\nless$ 60dB.
7) *Spurious Responses*
   $\nless$ −85dB.
8) *Frequency Stability*
   ±1·6kHz.
9) *Spurious Radiation at the Aerial*
   $\ngtr$ 200μV.

A specification requirement which offers particular difficulty is that relating to spurious responses. The permitted level of −85dB applies in the U.S.A. and Canada. For intermodulation, the German requirement of 60dB is the most stringent.

The above requirements may be divided roughly into two categories. First, there are those which are most dependent upon the performance of the active components used; this includes sensitivity, blocking, cross modulation, intermodulation. Second, there are those which are principally functions of circuit design and layout. The distinctions cannot, of course, be too rigidly drawn. For example, cross modulation and intermodulation arise from the non-linearities inherent in individual active components but are affected also by the a.g.c. action, which may be considered as a distributed circuit function in that it is affected by the performance of many stages, and in that freedom is available to the designer as to the manner in which he applies the reaction throughout the receiver.

RECEIVER BLOCK SCHEMATIC

An earlier proposal was a schematic approach to a design example of a 170MHz a.m. mobile communications receiver, based on the measured performance of the BF115 transistor as a v.h.f. mixer and on its estimated performance in other circuit functions. This first proposed schematic is shown in Fig. 1.

During the construction of an experimental receiver based on this proposal some modifications and improvements were adopted, for example

1) An improved noise—a.g.c. amplifier was proposed.
2) It was decided to improve front-end selectivity and to minimise spurious responses by an additional r.f. amplifier with a further modification to the a.g.c. system.
3) Two other local oscillator proposals were assessed; and one of these finally adopted.

The final block schematic is shown in Fig. 2.

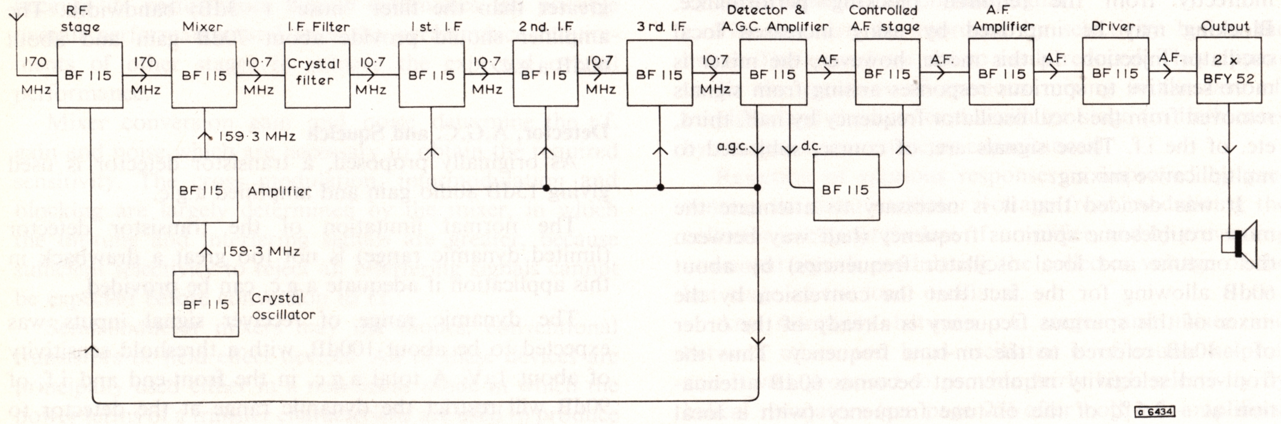

Fig. 1—First proposal for block diagram of 170MHz receiver

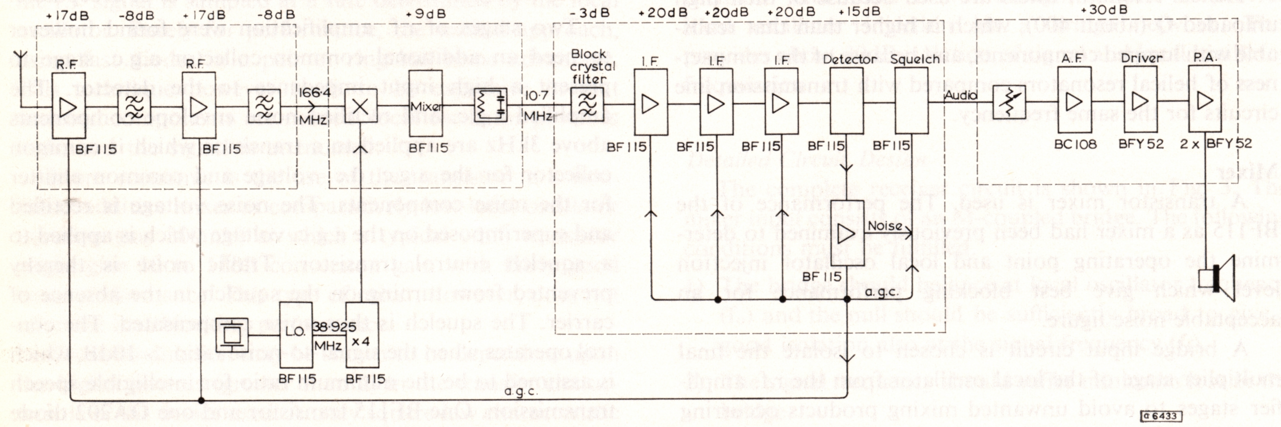

Fig. 2—Final block diagram of 170MHz receiver

General System Approach

A single conversion superheterodyne with a block crystal filter and i.f. of 10·7MHz was chosen for the following reasons:

1) Interfering signals would be removed from i.f. stages, easing the non-linear (cross modulation and blocking) requirements after the front-end.
2) The i.f. stages could be of comparatively wide bandwidth without tuning alignment and offer the possibility of later conversion to an integrated circuit form. (The cost of a suitable crystal filter is considered to be to some degree offset by the simplification of circuit construction and alignment and rather greater potential of miniaturisation of i.f. stages.)
3) There would be effectively no detuning of the i.f. stages with applied a.g.c.

R.F. Amplifier

It was accepted that front-end gain should be of the order of 30dB, of which about 12dB may be mixer conversion gain.

Two r.f. stages are used to provide the required gain (18dB) prior to the mixer, as well as to compensate for the insertion loss (16dB) of the interstage filters composed of twin-tuned under-coupled helical resonator pairs which are used to obtain image suppression and suppression of those spurious responses 5MHz or more away from the on-tune frequency.

The need to provide a high front-end selectivity arose indirectly from the required blocking performance. Blocking may be improved by using increased local oscillator injection. In this mode, however, the mixer is more sensitive to spurious responses arising from signals removed from the local oscillator frequency by half, third, etc. of the i.f. These signals are, of course, subjected to multiplicative mixing.

It was decided that it is necessary to attenuate the most troublesome spurious frequency (half way between the on-tune and local oscillator frequencies) by about 60dB allowing for the fact that the conversion by the mixer of this spurious frequency is already of the order of −40dB referred to the on-tune frequency. Thus the front-end selectivity requirement becomes 60dB attenuation at −3·5% of the on-tune frequency (with a local oscillator below the signal frequency).

Helical resonator filters are used because of their high unloaded Q (about 400), which is higher than that realisable with lumped components, and because of the compactness of helical resonators compared with transmission line circuits for the same frequency.

Mixer

A transistor mixer is used. The performance of the BF115 as a mixer had been previously examined to determine the operating point and local oscillator injection level which give best blocking performance for an acceptable noise figure.

A bridge input circuit is chosen to isolate the final multiplier stage of the local oscillator from the r.f. amplifier stages to avoid unwanted mixing products occurring before the mixer itself.

Local Oscillator

Subsequent to the originally proposed schematic, two further oscillator circuits were assessed. The first used a BFY52 oscillator-quadrupler followed by a BF115 buffer amplifier. The second used a BF115 oscillator and a BF115 quadrupler. The second of these circuits was chosen for the final schematic mainly because it uses only one inductor and is relatively simple to tune.

Block Filter

As previously proposed, a 10·7MHz i.f. was chosen. This frequency is high enough to ease the image rejection problem and is a standard frequency so that a readily available commercial crystal filter could be used.

I.F. Amplifier

The choice of a block filter to define the receiver selectivity permitted the choice of an i.f. amplifier without inductors. A wideband R-C coupled amplifier with some frequency selective feedback was proposed. This feedback reduces the noise contribution of the i.f. stages, but this contribution would not be large in any case with > 20dB r.f. gain (including the insertion loss of the crystal filter with its input and output matching networks).

The feedback is used more to help present a suitable load impedance to the crystal filter and to reduce the Miller shunting effect in individual stages.

The bandwidth of the i.f. amplifier itself would be much greater than the filter "nose" (−3dB) bandwidth. The amplifier should provide about 70dB gain and about 60dB a.g.c.

Detector, A.G.C. and Squelch

As originally proposed, a transistor detector is used giving 15dB audio gain and amplified a.g.c.

The normal limitation of the transistor detector (limited dynamic range) is not too great a drawback in this application if adequate a.g.c. can be provided.

The dynamic range of receiver signal inputs was expected to be about 100dB, with a threshold sensitivity of about 1μV. A total a.g.c. in the front-end and i.f. of 90dB will restrict the dynamic range at the detector to about 10dB, and a 10dB increase of audio output for a 100dB change of receiver input is assumed to be acceptable.

Two stages of r.f. amplification were found however to need an additional common collector a.g.c. stage to present a high input impedance to the detector. The amplified a.g.c. and rectified noise envelope components above 3kHz are applied to a transistor which is common collector for the a.g.c. d.c. voltage and common emitter for the noise components. The noise voltage is rectified and superimposed on the a.g.c. voltage which is applied to a squelch control transistor. Traffic noise is thereby prevented from turning on the squelch in the absence of carrier. The squelch is thus noise compensated. The control operates when the signal-to-noise ratio > 10dB, which is assumed to be the minimum ratio for intelligible speech transmission. One BF115 transistor and one OA202 diode are used in this squelch circuit.

Audio Amplifier

If a receiver sensitivity of 1μV (p.d. across 50Ω) is assumed, with a 30% modulated signal giving 50mW of audio power, and if about 100dB r.f. and i.f. gain is also assumed, then the audio stages (including the detector) should provide a gain equal to

$$10\log\left[\frac{5\times10^{-2}}{\left(\frac{(0{\cdot}3\times10^{-6})^2}{50}\right)}\right]-100 = 134{\cdot}5-100 \simeq 35\text{dB}.$$

Therefore, if the detector itself gives 15dB gain, the required audio gain is 20dB.

There is no standard requirement for the available audio power in commercial receivers. A 1W output is considered to be suitable with a reasonably efficient speaker for some mobile applications and can be provided by a transformerless class 'B' amplifier using inexpensive silicon transistors.

The audio amplifier complement is modified slightly from the original proposal in that a BC108 pre-amplifier, with higher specified gain than the BF115, eases the tolerancing of the amplifier over the temperature range (−20°C to +60°C), and over the voltage range (11V to 16·5V) and for more than the total gain spread of the BFY52 output transistor.

FRONT-END DESIGN

Mixer

The mixer is the first stage considered individually, because its performance largely determines the possible overall performance, and fixes the performance requirements of other stages to achieve the expected overall performance.

Mixer conversion gain and noise determine the r.f. gain and noise which are necessary to obtain the required sensitivity. The cross modulation, intermodulation and blocking are largely determined by the mixer, in which the on-tune and interfering signals are greater, because sufficient selectivity to reject all interfering signals cannot be expected before conversion to i.f.

Semiconductor mixers may use diodes, conventional transistors or field effect devices. All of these devices are principally used either in a non-linear mode in which the power terms of a transfer characteristic are used to produce sum and difference frequencies, or in an on-off mode wherein the r.f. signal is sampled at a rate determined by the local oscillator. Purely for performance, the second approach, using fast diodes in a pair or ring has some advantage. This technique however tends to be expensive in that matched components are needed, local oscillator power is high, and the signal is attenuated.

More economic is the use of the transistor in a non-linear additive mixer at comparatively low local oscillator injection (say 300mV) at which a typical v.h.f. transistor might give 10 to 11dB conversion gain with fairly good noise performance. This type of mixer, however, does not offer the best blocking performance.

Cross-modulation may be shown to be dependent upon the higher powers (greater than 2) in the transfer characteristic of the device used. A truly square-law characteristic such as is exhibited by field effect devices may be expected to be coupled with good cross-modulation performance. The field effect transistor is however at present considerably more expensive than the normal transistor.

It is to be expected that all non-linear mixers will show blocking because this is an effect which arises partly from the super-imposed linearising bias caused by large interfering signals.

The approach chosen was to use an inexpensive planar transistor (BF115) as a non-linear mixer working in a mode somewhat between the usual condition of large d.c. bias (compared with that due to local oscillator injection) and the pure on-off mode.

The empirical investigation to arrive at the required d.c. bias and local oscillator level showed that the local oscillator level of 700mV to 1V gave considerable benefit in blocking performance without undue increase of noise figure or decrease in gain. The interfering signal required to cause 3dB blocking (Ref. 1) under the chosen operating conditions can then be expected to be 130mV (p.d. across 50Ω). Thus 20dB r.f. gain before the mixer will still permit an input signal of 13mV to be applied without blocking. (This becomes 100mV if defined as in the G.P.O. specification where the interfering signal is expressed as a source e.m.f., with a source resistance of 75Ω, preceding a standard three-input star network.)

A further aspect of mixer performance is spurious responses which can be divided roughly into two types:

1) those 5MHz (approximately, for a 10·7MHz i.f.) or more away from the on-tune signal, and
2) those close to the on-tune signal.

The first can be improved by selectivity before the mixer. The second are not so easily reduced. They appear to be the products of spurious mixing in the last r.f. amplifier and the last local oscillator stage (in both cases by the non-linear collector capacitances).

Rejection of spurious responses is improved by preventing the local oscillator voltage from modulating the collector voltage of the last r.f. amplifier, and by preventing unwanted signals modulating the collector voltage of the last stage of the local oscillator.

Any selectivity between r.f. stages and mixer and between mixer and local oscillator is of course helpful, and it was proposed to provide fairly high selectivity by helical resonators (see page 22) after both r.f. amplifiers. Although these could also be used between the local oscillator and mixer it was thought simpler to provide local oscillator injection via a bridge network. This provides about 30dB isolation of signal and local oscillator frequencies.

Detailed Circuit Design

The complete receiver circuit is shown in Fig. 3. The mixer input consists of an M-coupled bridge. The following conditions must be fulfilled.

1) The bridge should balance at local oscillator frequency (f_o) and the null should be sufficiently broad to give a good isolation also at the signal frequency (f_i).
2) The signal frequency should suffer minimum loss in the bridge.

Condition (1) is satisfied by putting similar resistive and

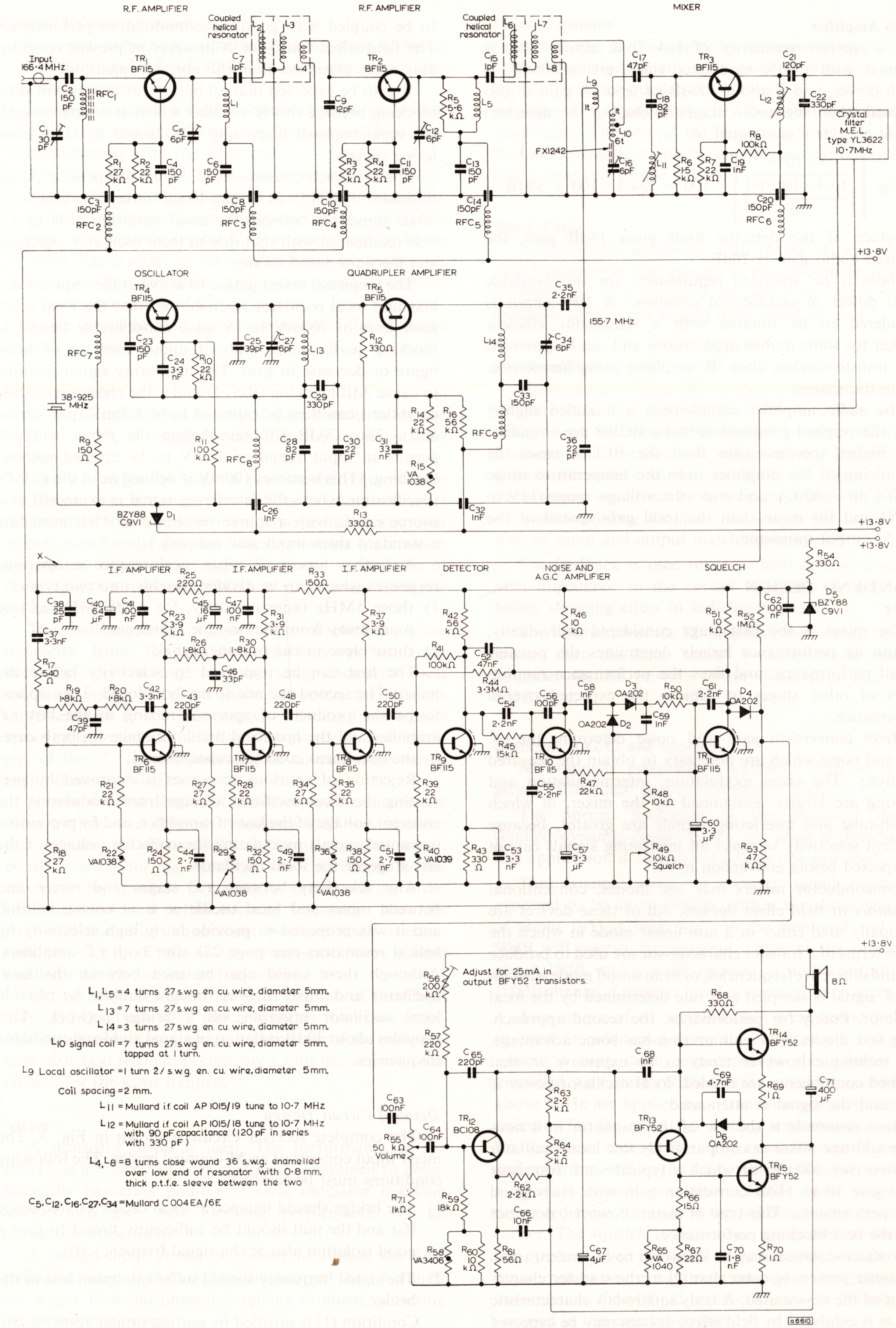
R.F. AMPLIFIER
R.F. AMPLIFIER
MIXER
Coupled helical resonator
Input 166·4MHz
Crystal filter M.E.L. type YL3622 10·7MHz
FX1242
+13·8V
OSCILLATOR
QUADRUPLER AMPLIFIER
155·7 MHz
38·925 MHz
BZY88 C9V1
I.F. AMPLIFIER
I.F. AMPLIFIER
I.F. AMPLIFIER
DETECTOR
NOISE AND A.G.C. AMPLIFIER
SQUELCH
Squelch
Adjust for 25mA in output BFY52 transistors
Volume
8Ω
L1,L5 = 4 turns 27 s.w.g. en. cu. wire, diameter 5mm.
L13 = 7 turns 27 s.w.g. en. cu. wire, diameter 5mm.
L14 = 3 turns 27 s.w.g. en. cu. wire, diameter 5mm.
L10 signal coil = 7 turns 27 s.w.g. en. cu. wire, diameter 5mm. tapped at 1 turn.
L9 Local oscillator = 1 turn 21 s.w.g. en. cu. wire, diameter 5mm.
Coil spacing = 2 mm.
L11 = Mullard i.f. coil AP 1015/19 tune to 10·7 MHz
L12 = Mullard i.f. coil AP 1015/18 tune to 10·7 MHz with 90 pF capacitance (120 pF in series with 330 pF)
L4,L8 = 8 turns close wound 36 s.w.g. enamelled over low end of resonator with 0·8 mm. thick p.t.f.e. sleeve between the two
C5,C12,C16,C27,C34 = Mullard C004EA/6E
E6610

Fig. 3—Circuit of complete receiver

reactive components in the two balance arms. Condition (2) is satisfied by making the two arms of the bridge unequal; thus the majority of f_i flows into the mixer input.

Fig. 4 shows a theoretical circuit of the bridge network. For analysis, it may be reduced to the circuit of Fig. 5a, in which

Z_a = input impedance of mixer transistor (assumed to be the same at f_i and f_o),

Z_b = corresponding balance impedance.

The leakage reactance between the local oscillator winding, L_o, and L_B, may be represented by the additional component L_e on the opposite side to L_o in Fig. 5b in which the transformed output impedance of the local oscillator is shown as Z_o.

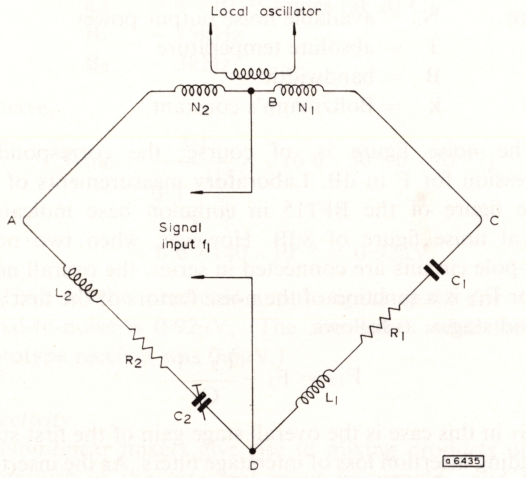
Local oscillator
N2
B
N1
A
C
Signal input fi
C1
L2
R2
R1
L1
C2
D
E6435

Fig. 4—Theoretical circuit of mixer bridge input

The circuit may be further analysed to make clear the factors controlling the attenuation of f_i. When the coupling between N_1 and N_2 is less than unity in the equivalent circuit shown in Fig. 5b, it may be redrawn as in Fig. 5c, in which Z_s is the source impedance of f_i (which is also the output impedance of the r.f. amplifier stage).

When the bridge is balanced, E_1 equals E_2 and we need consider only the open circuit four-pole network of Fig. 5d.

With the usual notation, we may write

$$E_1 = Z_{11}I_1+Z_{12}I_2 \qquad \ldots(1)$$

$$E_2 = Z_{21}I_1+Z_{22}I_2\,, \qquad \ldots(2)$$

where

$$Z_{11} = j\omega L_1+Z_s$$

$$Z_{22} = j\omega L_2+Z_s$$

$$Z_{12} = -j\omega M+Z_s$$

$$Z_{21} = -j\omega M+Z_s.$$

Also

$$M = k\sqrt{L_1L_2} \qquad \ldots(3)$$

$$I_s = I_1+I_2. \qquad \ldots(4)$$

At balance,

$$E_1 = E_2\,,$$

that is

$$Z_{11}I_1+Z_{12}I_2 = Z_{21}I_1+Z_{22}I_2$$

$$(Z_{11}-Z_{21})I_1 = (Z_{22}-Z_{12})I_2$$

$$\frac{I_1}{I_2}=\frac{Z_{22}-Z_{12}}{Z_{11}-Z_{21}}$$

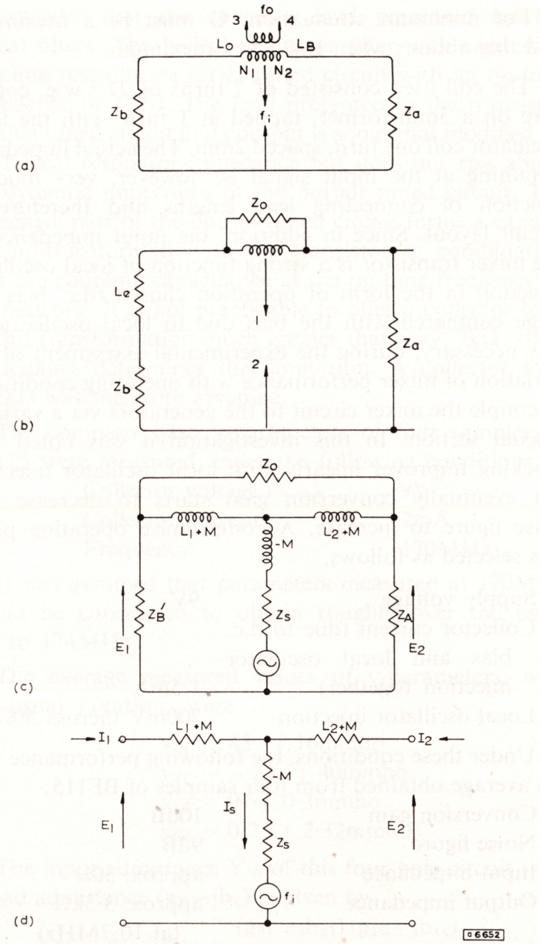
fo
3
4
Lo
LB
N1
N2
fi
Zb
Za
(a)
Zo
L2
1
2
Za
Zb
(b)
Zo
L1+M
L2+M
-M
Z'B
ZA
Zs
E1
E2
fi
(c)
I1
L1+M
L2+M
I2
-M
Is
E1
E2
Zs
fi
(d)
E6652

Fig. 5—Equivalent circuit of mixer bridge input

(a) Simple equivalent circuit
(b) Equivalent circuit with addition of leakage reactance and local oscillator output impedance
(c) Equivalent of 5(b) with coupling $N_1 : N_2 < 1$
(d) Four-pole equivalent of 5(c) with bridge balanced

or

$$\frac{I_1}{I_2}=\frac{j\omega(L_2+M)}{j\omega(L_1+M)}$$

$$=\frac{L_2+M}{L_1+M}. \qquad \ldots(5)$$

The attenuation, G, of f_i by the network, is given by the equation

$$G=\frac{I_2}{I_s}=\frac{I_2}{I_1+I_2}=\frac{1}{1+\frac{I_1}{I_2}}$$

that is

$$G=\frac{L_1+M}{L_1+L_2+2M} \qquad \ldots(6)$$

or

$$G=\frac{L_1+k\sqrt{(L_1L_2)}}{L_1+L_2+2k\sqrt{(L_1L_2)}}$$

$$=\frac{\frac{L_1}{L_2}+k\sqrt{\frac{L_1}{L_2}}}{1+\frac{L_1}{L_2}+2k\sqrt{\frac{L_1}{L_2}}}. \qquad \ldots(7)$$

For minimum attenuation, G must be a maximum, and this obtains when L_1/L_2 is a maximum.

The coil used consisted of 7 turns of 27 s.w.g. copper wire on a 5mm former, tapped at 1 turn, with the local oscillator coil one turn, spaced 2mm. The actual impedance obtaining at the input signal is, however, very much a function of connecting lead lengths and therefore of circuit layout. Since in addition, the input impedance of the mixer transistor is a strong function of local oscillator injection in the form of operation chosen (d.c. bias not large compared with the bias due to local oscillator) it was necessary, during the experimental assessment of the variation of mixer performance with operating conditions, to couple the mixer circuit to the generators via a variable coaxial section. In this investigation it was noted that blocking improves linearly with local oscillator injection but eventually conversion gain starts to decrease and noise figure to increase. A compromise operating point was selected as follows.

Supply voltage	9V
Collector current (due to d.c. bias and local oscillator injection together)	1·5mA
Local oscillator injection	700mV (across 50Ω)

Under these conditions, the following performance was the average obtained from four samples of BF115:

Conversion gain	10dB
Noise figure	9dB
Input impedance	approx. 30Ω
Output impedance	approx. 3·5kΩ (at 10·7MHz)
Blocking voltage (3dB loss in gain)	140mV (p.d. across 50Ω)

The i.f. output at 10·7MHz was to be applied to a crystal filter (M.E.L. type YL3622). The manufacturer's data on this component requires, for specified performance, that an impedance of 910Ω (±15%) in parallel with 25pF (±3pF) be seen by the filter at its input terminals. This impedance may be obtained by transforming the output impedance of the mixer transistor at 10·7MHz. Bearing in mind, however, the possible effect of component production spreads in aligning a receiver it was decided that the required impedance might be more simply obtained in the following manner.

1) A simple tuned impedance transformer is used to transform the mixer output resistance of about 3·5kΩ to 910Ω while allowing the output capacitance to be tuned.
2) A length (about 10cm) of 75Ω coaxial cable is used to connect the transforming circuit to the crystal filter. The capacitance of the particular line used is close to 25pF.

The front end may be tuned normally for maximum signal with a low capacitance detector and with the coaxial line disconnected. With the line re-connected the filter input is suitably terminated. The resistance transformation is conveniently made by a parallel tuned circuit with a capacitive tap.

R.F. Amplifier

Sensitivity

For a previously determined mixer noise figure, the overall receiver sensitivity becomes dependent upon pre-amplifier gain and noise. The proposed total front-end gain is sufficient to render the noise contribution of the i.f. amplifier negligible.

Representing the receiver as a noisy four-pole circuit of gain G, and noise factor F, we have

$$F = \frac{1}{G}\,\frac{N_o}{kTB}, \qquad \ldots(8)$$

where
N_o = available noise output power
T = absolute temperature
B = bandwidth
k = Boltzmann's constant.

The noise figure is, of course, the corresponding expression for F in dB. Laboratory measurements of the noise figure of the BF115 in common base indicate a typical noise figure of 8dB. However, when two noisy four-pole circuits are connected in series, the overall noise factor F_{12} is a function of the noise factors of the first and second stages, as follows.

$$F_{12} = F_1 + \frac{F_2 - 1}{G_1}. \qquad \ldots(9)$$

G_1 in this case is the overall stage gain of the first stage including insertion loss of interstage filters. As the insertion loss of tuned circuits rises, the loaded Q of the tuned circuits rises and the bandwidth falls in proportion. The practical limit is at an insertion loss of about 8dB, beyond which increased insertion loss shows a negligible increase of loaded Q. If the expected gain of an amplifier stage alone is 17dB, then

$$G_1 = 17 - 8 = 9\text{dB}. \qquad \ldots(10)$$

Therefore

$$F_{12} = 6{\cdot}25 + \frac{6{\cdot}25 - 1}{8} = 6{\cdot}6 = 8{\cdot}2\text{dB}. \qquad \ldots(11)$$

From this, the receiver sensitivity may be calculated. The noise voltage V_n developed at the input is given by

$$V_n = \sqrt{(F_{12} R_{in} kTB_1)} \qquad \ldots(12)$$

where
R_{in} = receiver input resistance (50Ω)
B_1 = total pre-detector bandwidth.

Callendar (Ref. 3) gives us the following relationship (for signal > noise) for different pre- and post-detector bandwidths.

$$\frac{V_{s(out)}}{V_{n(out)}} = m\frac{V_{s(in)}}{V_{n(in)}}\sqrt{\frac{B_1}{2B_2}} \qquad \ldots(13)$$

where
B_2 = post-detector bandwidth
m = modulation fractional index
$\frac{V_{s(in)}}{V_{n(in)}}, \frac{V_{s(out)}}{V_{n(out)}}$ = signal-to-noise ratio at input and output respectively.

From the G.P.O. Specification (Ref. 2),

$$\frac{V_{s(out)}}{V_{n(out)}} = 10\text{dB} = 3{\cdot}1 \text{ and } m = 0{\cdot}3$$

Therefore

$$V_{s(in)} = \frac{V_{s(out)}}{V_{n(out)}} \times \frac{V_{n(in)}}{m\sqrt{\left(\frac{B_1}{2B_2}\right)}}$$

$$= \frac{3{\cdot}1.\sqrt{(F_{12}R_{in}kTB_1)}}{0{\cdot}3\sqrt{\left(\frac{B_1}{2B_2}\right)}} \qquad \ldots(14)$$

Substituting values as follows,

F_{12} = 6·6
R_{in} = 50Ω
kT = 4×10^{-21} joules (at 20°C)
B_1 = 15kHz
B_2 = 3kHz

we have,

$$V_{s(in)} = \frac{3{\cdot}1}{0{\cdot}3\sqrt{\frac{15}{6}}} \times \sqrt{(6{\cdot}6\times50\times6\times10^{-17})}$$

$$= 6{\cdot}6\times140\times10^{-9} = 0{\cdot}92\mu\text{V}. \qquad \ldots(15)$$

That is, the predicted input signal (p.d.) for 10dB signal-to-noise is 0·92μV. (The measured value for the prototype receiver was 0·6μV.)

Selectivity

Non-linear mixers give rise to mixing products of the harmonics of the principal input frequencies, and have spurious responses to signals at the local oscillator frequency $f_o \pm \frac{1}{2}$, $\frac{1}{3}$, $\frac{1}{4}$, etc., of the i.f.

In a single ended mixer, the even terms predominate, and in particular the frequency $f_o \pm \frac{1}{2}$ i.f. may give a response above the specification level unless particular precautions are taken.

It was found that with a wider bandwidth pre-amplifier (about 4MHz) that the level of the spurious response was only −40dB relative to the on-tune frequency. It was deduced that the pre-amplification should have a selectivity characteristic about −60dB midway between the local oscillator and on-tune frequencies. This was confirmed by the design of interstage helical resonator filters with overall selectivity −65dB at that given frequency: the image rejection of the receiver then becomes better than −95dB and other spurious responses are also better than −90dB. It was in fact noted that the image response was unaffected whether or not the r.f. amplifiers were supplied with h.t., implying that the image is propagated by leakage.

Cross-modulation and intermodulation performance are considerably affected by a.g.c. action and so it was decided to apply full (and effectively non-delayed) reverse a.g.c. to the r.f. amplifier stages.

Detailed Circuit Design

It was decided to use the BF115 transistor in a common-base, unneutralised configuration as r.f. amplifier, and to achieve a stability factor of > 4 by resistive mismatch of the collector load. It was further decided to offer conjugate match to the input, which condition is sufficiently close to that for minimum (tuned input) noise figure.

Consider first the collector load presented by the helical filters. The helical resonator filter with capacitive coupling resembles a series tuned circuit with an on-tune impedance of 150Ω. The load presented to the transistor parallel tuned circuit at its output is somewhat modified by the helical resonator impedance but does not rise above the dynamic impedance of the output tuned circuit. The capacitive part of the output tuned circuit forms a capacitive up-transformation to the transistor in combination with the coupling capacitance at the on-tune frequency of the network. It is not practicable to offer a collector load by this transformation much greater than, say, 2kΩ: stray capacitance determines this limitation. A collector load of 2kΩ was therefore assumed.

The common base y-parameters of four samples of BF115 were measured under the following conditions:

Collector voltage (V_{cb})	9V
Collector current	2mA
Frequency	170MHz

It was assumed that parameters measured at 170MHz would be considered to obtain roughly over the band 156 to 174MHz.

The average measured values of y-parameters, with the usual notation, were

y_{11} = 45−j.16mmho
y_{21} = −23+j.40mmho
y_{12} = 0−j.0·3mmho
y_{22} = 0·2+j.2·32mmho

The input admittance Y_{in} of this four-pole circuit with a load admittance $(g_L + jb_L)$ is given by

$$Y_{in} = g_{11} + jb_{11} - \frac{(g_{21}+jb_{21})(g_{12}+jb_{12})}{(g_{22}+jb_{22})+(g_L+jb_L)}. \qquad \ldots(16)$$

For a tuned amplifier, it may be assumed, with small error, that

$$b_{22} + b_L \simeq b_{out} + b_L \simeq 0. \qquad \ldots(17)$$

Then we have

$$Y_{in} \simeq g_{11} + jb_{11} - \frac{(g_{12}g_{21} - b_{12}b_{21}) + j(b_{12}g_{21} + b_{21}g_{12})}{g_{22} + g_L}, \qquad \ldots(18)$$

whence

$$g_{in} = g_{11} - \frac{g_{12}g_{21} - b_{12}b_{21}}{g_{22} + g_L}. \qquad \ldots(19)$$

Inserting the appropriate values, and assuming a load of 2kΩ, we have

$$g_{in} = 45 - \frac{0{\cdot}3 \times 40}{0{\cdot}2 + 0{\cdot}5}\text{ mmho}$$

$$\simeq 28\text{mmho} \qquad \ldots(20)$$

and

$$b_{in} = b_{11} - \frac{b_{12}g_{21} + b_{21}g_{12}}{g_{22} + g_L}. \qquad \ldots(21)$$

Therefore

$$b_{in} = -16 - \frac{0{\cdot}3\times23}{0{\cdot}7} = -26\text{mmho}. \qquad \ldots(22)$$

For a conjugate match at the input, therefore, the source admittance $Y_s = (28 + j.26)$mmho.

We may then calculate Stern's stability factor (Ref. 4), which takes into account source and load admittance.

We may write

$$\text{Stability factor } K = \frac{2(g_{11}+g_s)(g_{22}+g_L)}{|Y_{12}Y_{21}|+\text{Re}[Y_{12}Y_{21}]} \qquad \ldots(23)$$

where $\text{Re}[Y_{12}Y_{21}]$ is the real part of $Y_{12}Y_{21}$.
Inserting the appropriate values gives

$$K = \frac{2(45+28)(0{\cdot}2+0{\cdot}5)}{13{\cdot}8+12} \simeq 4. \qquad \ldots(24)$$

A common base stage with 2kΩ load is therefore acceptably stable. We may calculate the power gain, G. of the amplifier from the expression

$$G = \left|\frac{Y_{21}}{Y_{22}+Y_L}\right|^2 . \frac{g_L}{g_{in}}. \qquad \ldots(25)$$

Inserting the appropriate values gives

$$G = \frac{2129}{0{\cdot}5} . \frac{0{\cdot}5}{28} = 76 = 18{\cdot}8\text{dB}. \qquad \ldots(26)$$

The total predicted r.f. gain before the mixer (allowing 8dB insertion loss for each of the two filters) then becomes

$$G_T = (18{\cdot}8\times2)-(8\times2) = 21{\cdot}6\text{dB} \qquad \ldots(27)$$

(As seen below the measured total r.f. amplification was approximately 18dB for one prototype front end).

The helical resonator filters used for front end selectivity are really special cases of the coaxial quarter-wave line, and extensive design information has been furnished by Zverev and Blinchikoff (Ref. 5). The inner conductor is coiled to form a helix, one end being earthed and the other open circuit. The helix is mounted in an outer container of pre-determined dimensions. Coupling into the resonator in this example is by capacitive probe, consisting of a length of p.v.c. insulated wire introduced axially into the helix from the earthed end. Coupling between first and second helixes of each pair is via an aperture at the high impedance ends. This is in effect, again, a capacitive coupling.

Coupling from the second helix to the following amplifier or mixer is by a coupling coil at the low impedance end of the second helix and this coil is externally capacitively tuned to offer the required Y_S (conjugate of Y_{in}) to the following stage.

In the design example, the details of the resonators are as follows, following the method and terminology of Zverev and Blinchikoff.

Filters to be double tuned with Butterworth response (two poles, no zeros) to allow correct alignment by nominal tuning techniques (tuning for maximum signal)

f_o	170MHz
Bandwidth (BW) (3dB)	1MHz (see note)
Insertion loss	8dB
q_{min} (Ref. 6) for Butterworth response for double tuned filter	1·4
Loaded $Q = Q_{min} = \dfrac{q_{min}\times f_o}{BW}$	238.

Note: The bandwidth of a tuned circuit is a function of loaded Q which is itself a function of unloaded Q. The unloaded Q of the helical resonator is strongly a function of the volume of the outer conductor (can) and increases with increasing can size.

The loaded Q of the resonator is strongly a function of coupling to source and load. Reducing this coupling increases the loaded Q at the expense of insertion loss.

However, as demonstrated by Zverev and Blinchikoff, there is little additional return for choosing a design insertion loss > 8dB.

We have, therefore, the following.

$$\text{Insertion loss } L = 20 \log_{10}\frac{U}{U-1} \text{ dB} \qquad \ldots(28)$$

where

$$U = \frac{\text{Unloaded Q}}{Q_{min}}.$$

That is,

$$20 \log_{10} \frac{U}{U-1} = 8,$$

whence

$$U = 1{\cdot}6$$

and

$$\begin{aligned}\text{Unloaded Q} &= U\times Q_{min}\\ &= 1{\cdot}6\times238\\ &= 381.\end{aligned}$$

To permit some tolerance on this figure, the resonators were designed for an unloaded Q of 400. The dimensions of the inner helix and outer conductor (Fig. 6) were

b = 14·5mm
d = 9·7mm
D = 14·5mm

The outer conductor was of square section. The coupling hole of 8·4mm diameter was drilled so as to extend from the inside edge of the top of the can. The cans were made of 1mm brass, plated 0·05mm with silver.

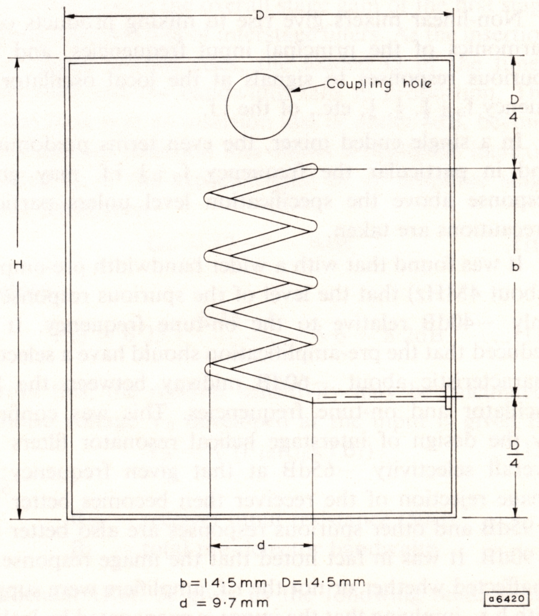

Fig. 6—Principal dimensions of one section one of the helical resonators

The helix consisted of 15·5 turns of copper wire, close wound, and of gauge chosen to fill the dimension 'b' (20 s.w.g.). Coil formers were of p.t.f.e. for minimum loss.

Fine tuning was accomplished by inserting a 4BA screw (silver plated brass) from the top of the can into the helix. The tuning adjustment is clearly quite sharp and care taken in the quality of mechanical components and assembly is essential. For this reason it might be observed that the p.t.f.e. formers used were not really considered sufficiently rigid.

In the prototype receiver, the resonator cans were soldered around the base to the brass screening box containing the front end.

Performance

The measured performance of the two r.f. amplifier stages constructed in cascade as shown in Fig. 3 may be summarized as follows.

Overall gain	18	dB
Overall noise figure	8·3	dB
Gain of each amplifier	17	dB
Noise figure of first amplifier	8	dB
Insertion loss of each filter	8	dB
Overall bandwidth (3dB)	800	kHz
Response +5MHz	−42	dB
Response −5MHz	−70	dB
Total consumption	4	mA
Supply voltage	13·8	V

Fig. 7 shows the overall response of the two r.f. amplifier stages. (In theory the image frequency should be attenuated 128dB. However, in a practical construction this is modified by leakage around coaxial plugs etc., and in fact attenuation ranging from 95dB to 117dB has been recorded.)

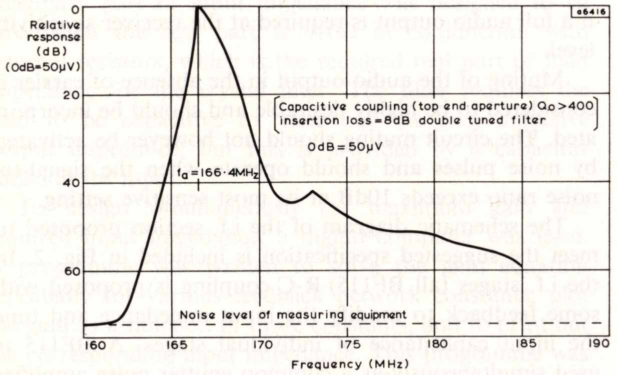

Fig. 7—Overall response of two-stage r.f. amplifier with two twin helical resonators

Local Oscillator

The original schematic proposed (Ref. 7) a local oscillator consisting of a transistor crystal controlled oscillator-quadrupler stage followed by a transistor buffer amplifier. A circuit designed and constructed to this proposal gave satisfactory performance. It was considered, however, that an oscillator which was simpler to tune would be attractive, and a further oscillator line-up was therefore considered using a BF115 crystal controlled oscillator at 38·925MHz followed by a BF115 as a quadrupler. A multiplication of four was chosen because a comparison was required with the first oscillator which was restricted in fundamental frequency. A higher fundamental frequency is however feasible with the second circuit (say 51·90MHz) followed by a trebler stage. Overall oscillator output should be improved thereby.

One particular restraint was placed upon the oscillator circuit itself in that it was considered of considerable advantage to earth one terminal of the crystal: this would be desirable in a multi-channel receiver with switched crystals.

As indicated on page 17, the oscillator is required to deliver, say, 700mV into 50Ω (10mW into the mixer) at 155·7MHz with a frequency stability (implied in the G.P.O. specification) against temperature variations, better than ±1·5kHz in the temperature range −10°C to +40°C.

Detailed Circuit Design

The oscillator circuit chosen might be considered to be 'common base' in that the feedback is applied from collector to emitter. The crystal is used in series mode feeding back from a tapping on the output tuned circuit to the emitter. A slight circuit rearrangement, however, allows one crystal terminal to be earthed with the common terminal floating.

Oscillator tuning consists only of adjusting the output tuning capacitor for maximum output since no frequency multiplication is now used in the oscillator.

The supply voltage of this stage is regulated by the voltage regulator diode to improve frequency stability with supply voltage variation.

A second BF115 is used in common base circuit capacitively coupled to the oscillator. The non-linear collector base capacitances enhance the performance as a frequency multiplier, in this case as a quadrupler. Harmonic generation is further improved by providing an additional tuned circuit at the input for the required harmonic. The output of the quadrupler is further capacitively coupled to the low impedance bridge input.

Performance

A prototype local oscillator had the following performance.

Supply voltage to multiplier	13·8	V
Regulated voltage supply to oscillator	(nominal) 9·1	V
Fundamental frequency	38·925	MHz
Output at fundamental frequency	18	mW
Output frequency	155·7	MHz
Output at 155·7MHz	10	mW
Frequency stability, −10°C to +40°C	±400	Hz
Frequency stability, 12V to 16V supply	(approx) 100	Hz

I.F. SECTION

The chief function of the i.f. amplifier in an a.m. receiver is to provide adequate drive for the detector. This means that signals at the sensitivity level of the receiver must be sufficiently amplified to drive the detector in a linear way. Therefore the performance of the detector, in conjunction with the performance of the front end, fixes the required i.f. amplification as well as audio amplification which follows it. A transistor detector has been chosen in preference to a diode detector for the present

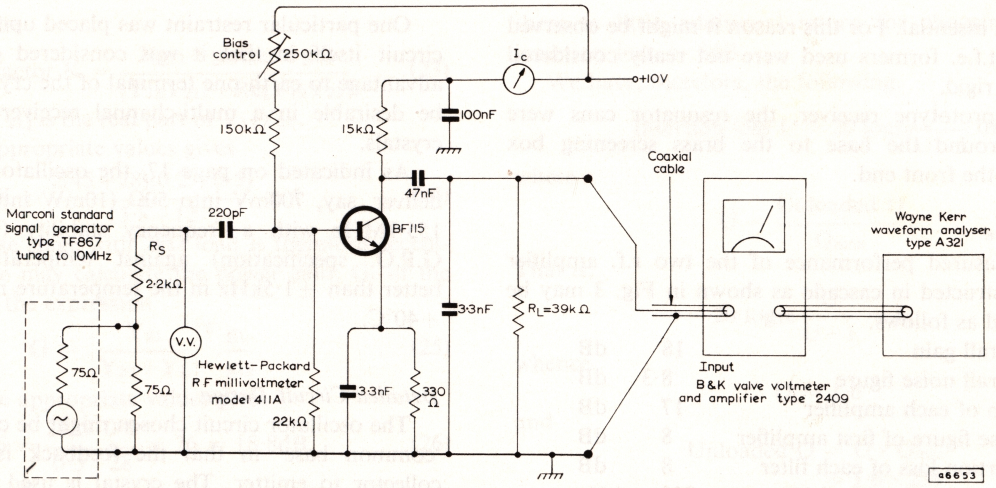
Bias control
250kΩ
150kΩ
15kΩ
I_c
+10V
100nF
47nF
Coaxial cable
Marconi standard signal generator type TF867 tuned to 10MHz
220pF
R_S
2·2kΩ
BF115
75Ω
75Ω
V.V.
Hewlett-Packard RF millivoltmeter model 411A
22kΩ
3·3nF
3·3nF
330 Ω
R_L=39kΩ
Input
B&K valve voltmeter and amplifier type 2409
Wayne Kerr waveform analyser type A321
a6653

Fig. 8—Test circuit for measurement of demodulation distortion

design for the following reasons:

1) A.F. feedback within the transistor can be used to linearise demodulation at relatively low signal level.
2) Some audio gain and amplified a.g.c. voltage can be provided by the detector.
3) The input impedance of the transistor detector offers a convenient direct match to the last i.f. stage.

The disadvantage of a transistor detector compared with the diode detector is its limited dynamic range. In a communications receiver with effective a.g.c., this is not a serious drawback. Investigations were carried out on the BF115 transistor used as a detector, and from the data obtained, it was decided that a signal of 50mV r.m.s. is required as the input to the detector for satisfactory demodulation. The test circuit in which percentage modulation distortion was measured is given in Fig. 8.

A 60% modulated 50mV signal was shown to undergo about 8% harmonic distortion. However in conjunction with the last i.f. stage, the even harmonic distortion partly cancels that in the detector, and much lower system distortion is actually achieved.

Receiver sensitivity is defined by the noise factor and gain of the front end. The front end of the present design provides an input sensitivity of 0·6μV for 10dB signal-to-noise ratio and a gain of 28dB. The block crystal filter has an insertion loss of 3dB, bringing the total pre-i.f. gain to 25dB.

The required i.f. gain ($G_{\text{i.f.}}$) is therefore given by the equation,

$$G_{\text{i.f.}} = \left(20\log\frac{50\times10^{-3}}{0{\cdot}6\times10^{-6}} - 25\right)\text{dB} = 73{\cdot}4\text{dB} \quad \ldots(29)$$

Three stages of direct coupled wideband i.f. amplification would be needed for this order of gain.

A 50mV 30% modulated signal to the detector gives an audio output signal of 160mV r.m.s. Considering the audio amplifier, the output voltage to the loudspeaker will always be less than $(13{\cdot}8/2)\times0{\cdot}707 = 4{\cdot}8$V r.m.s. as a result of output transistor saturation.

In practice an output voltage of 3·5V r.m.s. may be assumed. The total audio gain, G_a, required after detection is, therefore

$$G_a = 20\log\left(\frac{3{\cdot}5}{0{\cdot}16}\right) = 27\text{dB}, \quad \ldots(30)$$

if a full audio output is required at the receiver sensitivity level.

Muting of the audio output in the absence of carrier is considered to be highly desirable and should be incorporated. The circuit muting should not however be activated by noise pulses and should operate when the signal-to-noise ratio exceeds 10dB at its most sensitive setting.

The schematic diagram of the i.f. section proposed to meet the suggested specification is included in Fig. 2. In the i.f. stages (all BF115) R-C coupling is proposed with some feedback to modify the input impedance and tune the input capacitance of individual stages. A BF115 is used simultaneously as a common emitter noise amplifier for the squelch and as a common collector a.g.c.amplifier. A further BF115 provides muting. The audio amplifier uses BFY52 n-p-n transistors as a transformerless output stage for an 8Ω loudspeaker. The detailed circuit diagram of the i.f. and audio section is included in Fig. 3.

I.F. Amplifier Design

The basic requirement for the design of this i.f. was that the use of inductors should be avoided altogether in the interests of compactness. In general, this would mean that stages would have low gain because;

1) the real part of load and source impedance would not be matched;
2) Miller effect and input capacitance would shunt the input of each stage capacitively.

In the absence of inductive transformers, little can be done about (1), and some mismatch of load and source impedance must be accepted. But input capacitance and Miller capacitance can be cancelled out by a suitable feedback network.

In the terminology of the general y-parameter equivalent circuit, the source susceptance, b_s, presented to a transistor stage should be the input susceptance, b_{in}, of that stage, that is

$$b_s = -b_{in}.$$

Reference to Figs. 3 and 9 shows the form of feedback network which was chosen to meet this requirement. The feedback network allows b_{in} to lie in the required range and it may in fact be positive or negative.

In the optimum case a single BF115 stage can give a power gain of 25dB as compared with about 17dB for the untuned case. The first two i.f. stages have had their input impedance modified in this way. In the first stage the imaginary part of input impedance was designed to be zero when the real part is 910Ω in conjunction with external resistors, which is the required real part of load impedance for the crystal filter. The filter requires the load to be capacitive to 'tune out' its own inductive output impedance, but this is provided by a capacitor added at the input.

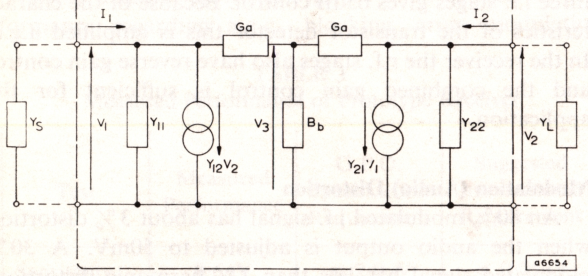

Fig. 9—Four-pole circuit with added feedback network

To design simultaneously for maximum gain and required input impedance, a digital computer was used. A programme was written to solve the gain equation repeatedly for various feedback network constants, plot the gain as a function of those constants, and to print out the corresponding input impedance. This programme was used to give an overall idea of the effect of the feedback network and the effect of varying constants, and to note the occurrence of maximum independent functions.

A further and shorter programme was used to obtain the feedback network constants for maximum gain conditions only, when one of two feedback network parameters was varied. Input impedance, gain and Stern's stability factor, K, were also printed out.

A preliminary calculation showed that the first stage could not itself provide a high enough load impedance for the crystal filter and so a series resistor was included to obtain a proper match.

A final computation provided feedback network constants for maximum gain.

An analysis is given below of an active four-pole circuit used in the i.f. amplifier.

Circuit Analysis of Single Stage

The first and second i.f. amplifier transistors are shunted by an R-C shunt feedback network as shown in Fig. 3. Fig. 9 represents an active four-pole circuit with such a network added. This circuit can be represented also by a four-pole circuit with modified parameters; the usual gain and input admittance formula may then be applied to this modified circuit. To obtain the modified y parameters, we have,

$$I_1 = V_1y_{11}+V_2y_{12}+(V_1-V_3)G_a \quad \ldots(31)$$

$$I_2 = V_2y_{22}+V_1y_{21}+(V_2-V_3)G_a \quad \ldots(32)$$

$$V_3jB_b = (V_1+V_2-2V_3)G_a \quad \ldots(33)$$

From Eq. 33

$$V_3 = (V_1+V_2)\left(\frac{G_a}{2G_a+j.B_b}\right) \quad \ldots(34)$$

Substituting in Eqs. 31 and 32 gives, therefore,

$$I_1 = V_1\left(y_{11}+G_a-\frac{G_a^2}{2G_a+j.B_b}\right)+V_2\left(y_{12}-\frac{G_a^2}{2G_a+j.B_b}\right) \quad \ldots(35)$$

$$I_2 = V_2\left(y_{22}+G_a-\frac{G_a^2}{2G_a+j.B_b}\right)+V_1\left(y_{21}-\frac{G_a^2}{2G_a+j.B_b}\right). \quad \ldots(36)$$

If this circuit has the modified y-parameters y_{11}', y_{22}', y_{21}', y_{12}', then,

$$y_{11}' = y_{11}+G_a-\frac{G_a^2}{2G_a+j.B_b} \quad \ldots(37)$$

$$y_{22}' = y_{22}+G_a-\frac{G_a^2}{2G_a+j.B_b} \quad \ldots(38)$$

$$y_{21}' = y_{21}-\frac{G_a^2}{2G_a+j.B_b} \quad \ldots(39)$$

$$y_{12}' = y_{12}-\frac{G_a^2}{2G_a+j.B_b}. \quad \ldots(40)$$

The input admittance Y_{in}, of the circuit with load admittance Y_L, is given by

$$Y_{in} = y_{11}+G_a-\frac{G_a^2}{2G_a+j.B_b} - \left(\frac{\left(y_{21}-\frac{G_a^2}{2G_a+j.B_b}\right)\left(y_{12}-\frac{G_a^2}{2G_a+j.B_b}\right)}{y_{22}+G_a-\frac{G_a^2}{2G_a+j.B_b}+Y_L}\right) \quad \ldots(41)$$

This value of Y_{in}, together with the admittance of appropriate collector load resistor, is the value of Y_L offered to the first i.f. amplifier stage by the second.

The available stage power gain, P, is given by

$$P = \frac{4.G_s.G_L.|y_{21}'|^2}{|y_{22}'+Y_L|^2\times|Y_{in}+Y_s|^2} \quad \ldots(42)$$

Stern's stability factor, K, is given by the equation

$$K = \frac{2(g_{11}'+G_s)(g_{22}'+G_L)}{|y_{12}'y_{21}'|+\text{Re}[y_{12}'y_{21}']} \quad \ldots(43)$$

The stage is unconditionally stable if $K > 1$ for the given loading condition. The four y-parameters for the BF115 transistor used are needed and are as follows at $f = 10{\cdot}7$MHz, $I_C = 2$mA. (All units are in μmho.)

$$y_{11} = 800+j.2500$$

$$y_{22} = 4{\cdot}5+j.82$$

$$y_{12} = 0-j.30$$

$$y_{21} = 59\,500-j.10\,000.$$

If a collector resistor of 3·9kΩ is used, then

$$Y_L = Y_{in}+\frac{10^3}{3{\cdot}9} = G_{in}+\frac{10^3}{3{\cdot}9}+j.b_{in}\text{mho} \quad \ldots(44)$$

The actual value is a little higher because of biasing resistors in parallel. The value of $j.b_{in}$ is very small because of the feedback network, and may be neglected. When the crystal filter is used as the source, the imaginary parts are tuned out by the input capacitor and

$$Y_S = \frac{10^6}{910}\ \mu\text{mho} \qquad \ldots(45)$$

The value of Y_S is actually smaller because of the series resistor used to match it to the load (540Ω). The computer programmes in Algol for the Elliott 503 digital computer are included in Appendix 1. Specimen plotted results are shown in Fig. 14. The component values thus obtained are included in the circuit diagram (Fig. 3).

Detector and Squelch

The transistor used as a detector is operated at a quiescent current of about 100μA. The presence of signal causes the quiescent current to rise. The voltage at the collector is used to derive base bias for the i.f. and r.f. transistors; signal on the detector causes the i.f. and r.f. current to fall, reducing gain and providing reverse a.g.c. The squelch circuit operates from the a.g.c. voltage, but noise components at the output of the detector above 4kHz are amplified and used to inhibit squelch operation until the bias due to carrier exceeds the bias due to noise.

Sensitivity

The i.f. amplifier constructed has a measured noise figure of 11dB. The bandwidth excluding the crystal filter is 7MHz centred on 10·7MHz. Taking a post-detector bandwidth of 3kHz, the p.d. $V_{s(in)}$ at the input (Point X in Fig. 3) to give a 10dB signal-to-noise ratio is:

$$V_{s(in)} = \frac{3{\cdot}1 \times \sqrt{(FRkTB_1)}}{m\sqrt{\left(\dfrac{B_1}{2B_2}\right)}} \qquad \ldots(46)$$

Where m = modulation depth.

B_1 and B_2 are pre- and post-detection bandwidths (7MHz, 3kHz respectively).

F = i.f. noise factor

R = input resistance of amplifier, predicted to be 910Ω as required to match the crystal filter

kT = a constant which at 20°C = 4×10^{-21} joules.

Therefore

$$V_{s(in)} = \frac{3{\cdot}1 \times \sqrt{(12{\cdot}6 \times 910 \times 7 \times 10^6 \times 4 \times 10^{-21})}}{0{\cdot}3 \times \sqrt{\left(\dfrac{7 \times 10^6}{2 \times 3 \times 10^3}\right)}} = 5{\cdot}3\mu\text{V}. \qquad \ldots(47)$$

This order of sensitivity is sufficient to ensure that the sensitivity of the receiver is not affected by the i.f. section and is defined by the performance of the front end.

Gain

The overall voltage gain was measured as 84dB between the point 'X' (Fig. 3) and the detector output.

Selectivity

The selectivity of the i.f. amplifier excluding the crystal filter is not great, but both the high pass R-C coupling between stages and the selective feedback techniques reduce the bandwidth to about 7MHz and this is sufficient to render the noise contribution of the first stage of the i.f. negligible. The overall selectivity of the i.f. amplifier is effectively the bandwidth of the crystal filter at the input and is 15kHz.

A.G.C.

Reverse bias automatic gain control applied over all three i.f. stages gives 65dB control. Because of the characteristics of the transistor detector this is amplified a.g.c. In the receiver the r.f. stages also have reverse gain control and the combined gain control is sufficient for the application.

Modulation (Audio) Distortion

An 80% modulated i.f. signal has about 3% distortion when the audio output is adjusted to 50mV. A 30% modulated signal has less than 1% harmonic distortion, at receiver input levels under 500μV.

The third i.f. amplifier stage has no external feedback network because the detector which follows it must be fed from as high a source impedance as possible to reduce audio distortion. As indicated previously a transistor detector was chosen. The detector is followed by a noise compensated squelch circuit which passes the audio signal as soon as the input carrier exceeds input and receiver noise by 10dB. It has negligible hysteresis because of a small amount of d.c. positive feedback to the detector input via a 3·3MΩ resistor.

AUDIO SECTION

It was decided to complete the design with a 1W output stage, and a transformerless design was considered. Of a number of possible configurations the one needed to have the following characteristics:

1) little change in quiescent current for changes of battery voltage,
2) little change of mid-point voltage with change of battery voltage,
3) operation from −10 to +60°C.

The circuit configuration chosen for the design is relatively simple and economic and its performance is a compromise between (1) and (2) above. Operation is up to +60°C and 1·2W audio output is available with a supply voltage of 13·8V.

SUMMARY OF OVERALL RECEIVER PERFORMANCE

A prototype receiver was constructed according to the circuit diagram in Fig. 3. Numerous sub-assemblies were also constructed and individually tested. The complete receiver was also subjected to tests as defined in the relevant G.P.O. Specification (Ref. 2). The measured performance of the complete receiver and certain aspects of the performance of sub-assemblies are given in Table 1. The receiver met the requirements of the specified tests and on most points also met the suggested requirements (page 15) of all other countries.

The voltages are expressed as p.d. across the (50Ω) receiver input. Tests were made except where otherwise stated at normal room temperature and at d.c. supply voltage of 13·8V.

It is seen that the most difficult requirements were found to be blocking and intermodulation. In fact, the prototype receiver did not meet fully the requirements of all countries regarding intermodulation.

More detail is shown in Figs. 10 to 13 of receiver performance regarding a.g.c., blocking, cross modulation

TABLE 1

Measured Performance of Prototype Receiver

Test	Measured Performance	G.P.O. Specification Requirement	Suggested 'International' Requirement
Sensitivity	0·6μV (Signal-to-noise 10dB)	⩽ 2·0μV (Signal-to-noise 10dB)	⩽ 0·75μV (Signal-to-noise 12dB)
A.G.C.	⩽ +10dB change of output for up to 200mV signal input	—	—
Nose Band-width (−3dB)	15kHz	—	⩾ 12kHz
Selectivity (> 23·5kHz off tune)	90dB	⩾ 70dB	⩾ 70dB
Image rejection	95dB	⩾ 70dB	⩾ 70dB
Other spurious responses	> 90dB	⩾ 70dB	⩾ 85dB
Blocking	18mV	≮ 13·3mV	—
Cross Modulation	35dB	≮ 30dB	—
Inter-modulation	55dB	≮ 50dB	≮ 60dB
Frequency Stability (−10°C to +40°C)	±400Hz	(Note (i))	±1·6kHz
Radiation at Aerial Terminals	11μV	<20nW (Note (ii))	<200μV

Note (i) A frequency stability of ±1·5kHz in the given temperature range is implied.
(ii) The given power corresponds to 1mV across 50Ω, or a source e.m.f. (50Ω source) of 2mV.

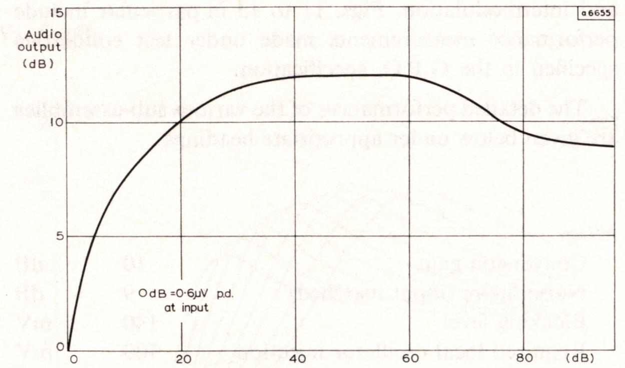

Fig. 10—A.G.C. characteristics of complete receiver

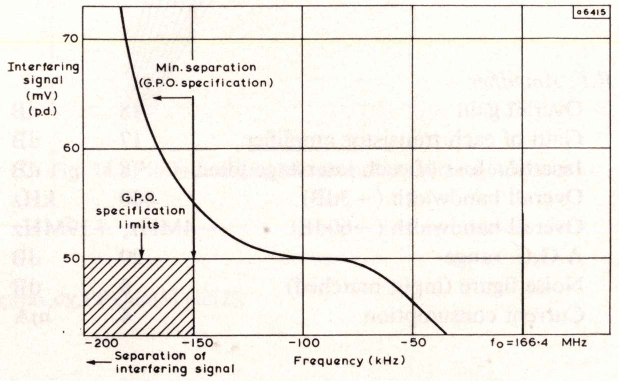

Fig. 11—Blocking curve of receiver

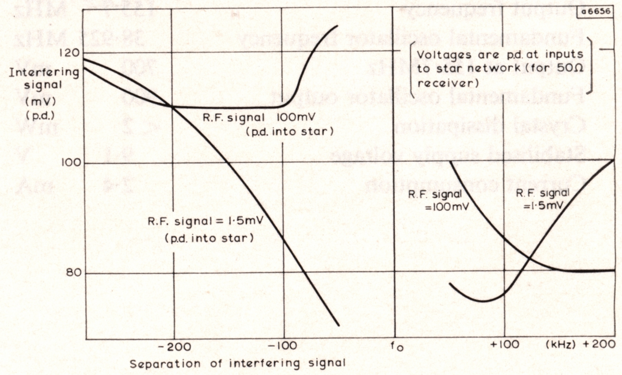

Fig. 12—Cross-modulation of receiver

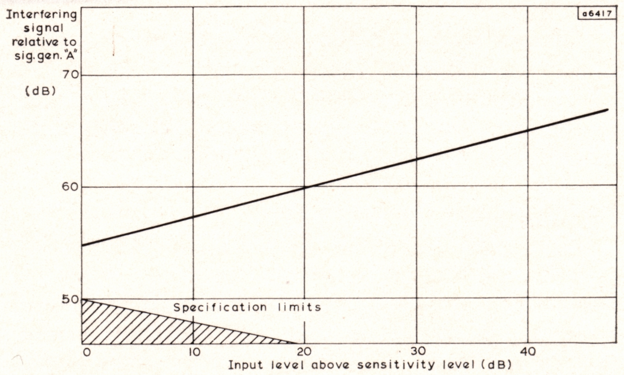

Fig. 13—Receiver intermodulation versus signal level

and intermodulation. Figs. 11 to 13 in particular include performance measurements made under test conditions specified in the G.P.O. specification.

The detailed performances of the various sub-assemblies are given below under appropriate headings.

Mixer

Conversion gain	10	dB
Noise figure (input matched)	9	dB
Blocking level	140	mV
Required local oscillator injection	700	mV
Current consumption	1·6	mA
Impedance presented to crystal filter	910 in parallel with 25pF	Ω

R.F. Amplifier

Overall gain	18	dB
Gain of each transistor amplifier	17	dB
Insertion loss of each interstage filter	8	dB
Overall bandwidth (−3dB)	800	kHz
Overall bandwidth (−60dB)	−4MHz, +19MHz	
A.G.C. range	20	dB
Noise figure (input matched)	8	dB
Current consumption	4	mA

Local Oscillator

(Receiver on-tune frequency = 166·4MHz)

Output frequency	155·7	MHz
Fundamental oscillator frequency	38·925	MHz
Output at 155·7MHz	700	mV
Fundamental oscillator output	900	mV
Crystal dissipation	< 2	mW
Stabilised supply voltage	9·1	V
Current consumption	2·4	mA

I.F. Amplifier, A.G.C. Amplifier and Detector

Overall voltage gain	84	dB
Input impedance presented to crystal filter	910 in parallel with 25pF	Ω
A.G.C. range	> 60	dB
Audio output (for 7μV input) 30% modulation	approx 50	mV

Audio Amplifier

Overall voltage gain	30	dB
Maximum output power (13·8V supply)	1·2	W
Maximum output power (12V supply)	1	W
Maximum output power (16V supply)	1·3	W
Total distortion (1W)	< 2	%
R_L (Loudspeaker impedance)	8	Ω

Squelch

Minimum signal to operate	0·6	μV

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APPENDIX I

Gain and Stability calculation for various values of Y_s, Y_L, G_a, B_b

```
     real procedure modsq(x); array x;
     modsq:=x[1]*x[1]+x[2]*x[2] ;
     procedure prelim(g,b) ;
     value g,b; real g,b;
     begin real u,v,w ;
                w:=b*b; u:=g*g; v:=4*u+w ;
                x[1]:=2*u*g/v; xx[1]:=g+x[1];
                xx[2]:=x[2]:=−u*b/v;
                U(S(T(ylp),T(xx)),zl) ;
                U(N(T(y21),T(x)),z21);
                U(N(T(y12),T(x)),z12);
                U(P(T(z12),T(z21)),z12);
U(N(S(T(y11),S(T(xx),T(xx))),Q(T(z12),T(zl))),yin) ;
end prelim ;
real procedure RYIN(g,b); value g,b; real g,b;
begin prelim(g,b); RYIN:=yin[1] end ;
real procedure IYIN(g,b); value g,b; real g,b;
begin prelim(g,b); IYIN:=yin[2] end ;
data: for k:= 1,2 do read ys[k],yl[k],y11[k],y12[k],y21[k],y22[k] ;
read gmin,gmax,dg,bmin,bmax,db ;
  comment in mumhos ;
k:= 0; U(S(T(yl),T(y22)),ylp) ;
U(S(T(ys),T(y11)),ysp) ;
for b:=bmin step db until bmax do
begin print scaled(6),b,prefix(££s2??),bisec(IYIN(g,b)+ys[2],g,gmin,gmax,dg,PP),yin[1],yin[2],
U(S(T(yin),T(ys)),x); print scaled(5),prefix(££s2??),
4*ys[1]*yl[1]*modsq(z21)/(modsq(zl)*modsq(x)),
2*(ysp[1]+xx[1])*zl[1]/(z12[1]+sqrt(modsq(z12)));
end;
  goto data;
PP: for g:=gmin step .1*(gmax−gmin) until gmax+dg do print IYIN(g,b); goto data;
QQ: RR:
end;
```

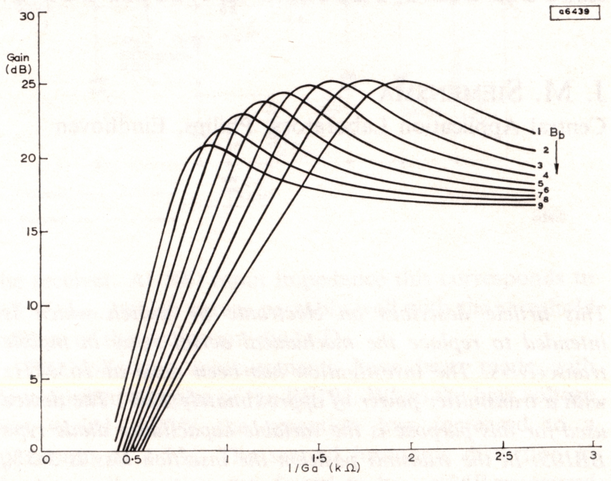


Fig. 14—Plotted output of computer gain calculations

Electronic Aerial Switch for Mobile Transceivers

J. M. SIEMENSMA
Central Application Laboratory, Philips, Eindhoven

This article describes an electronic t-r switch which is intended to replace the mechanical aerial relay in mobile transceivers. The investigation has been done at 165MHz with a transmitter power of approximately 12W. The device used for this purpose is the variable capacitance diode type BB105. In the transmit position the insertion loss is 3·3% (power) of which only 6mW is delivered to the receiver. The current consumption in this position is 20mA at 13·8V. In the receive position the insertion loss is 3·5% (power).

INTRODUCTION

A description is given in this article of a solid state circuit that switches the aerial from transmitter to receiver, and vice versa. It is intended for mobile transceivers in the 160MHz band with a transmitting power of about 12W.

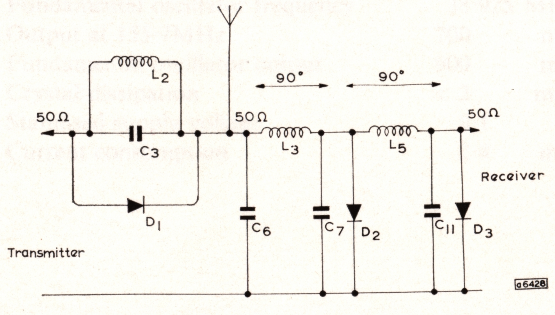


Fig. 1—Simplified circuit diagram of aerial switch

The solid state t-r switch is the first step to the elimination of all mechanical relays in mobile transceivers. Its advantages are higher reliability at the same or lower cost, less power consumption, and automatic protection of the receiver against a too high input voltage.

DESCRIPTION OF CIRCUIT

Fig. 1 gives a simplified circuit diagram of the switch, in which the bias provisions are not shown. When the transmitter is operating, the diodes D_1 and D_2 are forward biased and present only a small resistance. During reception, D_1 and D_2 are reverse biased, and present a high-Q capacitance. The diode D_3 (BAY38) has zero bias in both cases. During transmission D_1 short circuits the circuit L_2C_3, so that the transmitter signal reaches the aerial.

The diode D_2 also forms a short circuit, but the 90° low-pass network transforms this short circuit to an open circuit at the aerial. Because D_2 is not an ideal short circuit, some transmitting power will leak through and reach the receiver. This power is limited by diode D_3, which becomes conducting as soon as the r.f. voltage exceeds approximately $0{\cdot}5V_{r.m.s.}$. During reception L_2,C_3 and D_1 form a parallel-tuned circuit, blocking the transmitter from the aerial. The received signal can reach the receiver via the two low-pass sections. When the signal exceeds approximately $0{\cdot}5V_{r.m.s.}$, the diode D_3 becomes conducting and clips the signal.

Fig. 2 shows the complete circuit diagram. To keep the power consumption low, the diodes are put in series for d.c. flow. The d.c. path is R_1, L_1, D_1, L_3, D_2, and L_4, while the capacitors C_1, C_2, C_5, C_8 and C_{10} are d.c. blocking capacitors. The bias voltage is 13·8V for transmitting as well as receiving. Switching from transmit to receive and vice versa is achieved by reversing the polarity of the bias voltage. In the transmit position, a forward current flows through the diodes, and is chosen to be 20mA by means of R_1. Although an r.f. current of about $0{\cdot}5A_{r.m.s.}$ flows through the diodes, this low d.c. current of 20mA is sufficient because the periodic time of the r.f. current is very small with respect to the reverse recovery time of the diode, and so the r.f. current is flowing mainly through the diffusion capacitance.

In the receive position the diodes are reverse biased; the bias voltage being equally divided between R_2 and R_3. The r.f. choke L_6 completes the d.c. path for diode D_3.

PERFORMANCE

Measurements have been made at 165MHz. All diodes have been measured with a 100pF capacitor in series, and Table 1 shows the results obtained for three samples of the diode BB105.

The BAY38 which is used here as protection diode showed the following parameters: $V_D = 0$, $c_D = 0{\cdot}5$pF, $R_p = 15$kΩ at f = 165MHz.

It was decided that a maximum insertion loss of 5% is acceptable both for transmitting and for receiving and it has been found that the BB105 meets this requirement. The BB105 in this circuit gives a power insertion loss of 3·3% in the transmit position, and 3·5% in the receive position. In the transmit position a power of 6mW reaches the receiver. At 50Ω input impedance this corresponds to $0{\cdot}55V_{r.m.s.}$, which agrees passably well with the threshold voltage of the protection diode D_3.

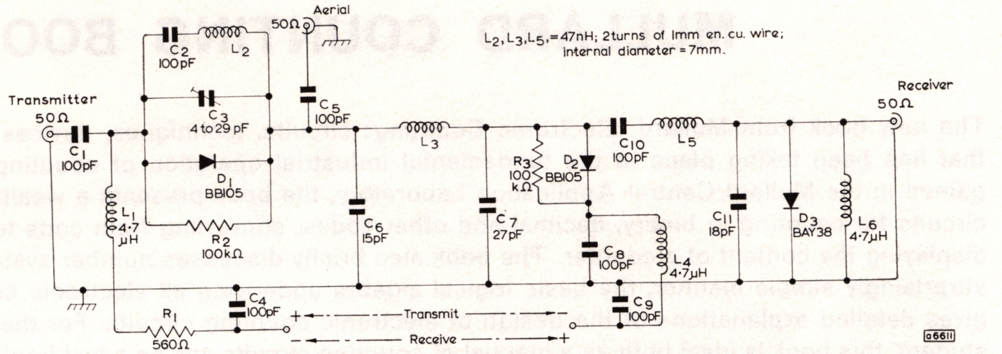


Fig. 2—Full circuit of aerial switch

TABLE 1

Parameters of BB105 at 165MHz

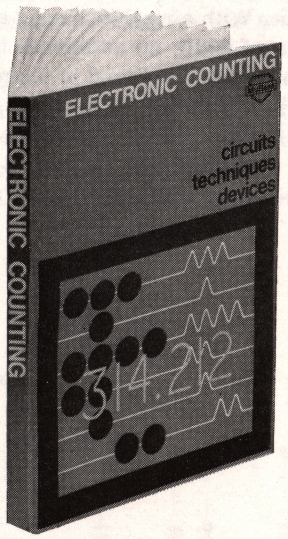
Sample of BB105	R_s (Ω) at $I_F = 20$mA	c_D (pF) at $V_R = 7{\cdot}0$V	R_p (kΩ) at $V_R = 7{\cdot}0$V
1st	0·41	6·5	40
2nd	0·49	6·23	36
3rd	0·47	5·5	28

The following measurements have been made with development samples of the BB105. When the bias voltage was varied ±20% the reception loss increased to a maximum of 4·5%. The second harmonic distortion in the transmit position was found to be −68dB measured with an input signal having 95dB suppression of the second harmonic. With a receiver having an intermodulation suppression of 60dB, no additional intermodulation due to the aerial switch was found in the receive position.

MULLARD COUNTING BOOK

The new book from Mullard 'Electronic Counting: circuits, techniques, devices' reflects the revolution that has been taking place in the fundamental industrial operation of counting. Based on experience gained in the Mullard Central Application Laboratory, the book presents a wealth of practical electronic circuits for counting in binary, decimal and other codes, converting from code to code, and storing and displaying the content of a counter. The book also briefly discusses number systems and describes, in a surprisingly simple manner, the basic logical algebra underlying all electronic counting equipment, and gives detailed explanations of the design of electronic counting circuits. For the design engineer or the student, this book is ideal both as a manual of counting circuits and as a text book on electronic counting.

Features of the book are as follows. It gives the theory and practice of electronic counting, presents a simple approach to Boolean algebra, describes and analyses basic counting elements, and gives comprehensive coverage of practical circuits for binary, binary-coded-decimal, ring and modulo-n counters. It also considers both gasfilled and solid-state counting devices, including discrete-component and integrated-circuit executions of the practical counters, and covers storage and display circuits and devices.



Chapter-by-chapter Description

Chapter 1—INTRODUCTION
The concept of numbers is briefly outlined, and codes relating the decimal and binary systems of numbers are introduced.

Chapter 2—THE LANGUAGE OF LOGIC
A simple explanation of the application of logic to switching circuits is given.

Chapter 3—BASIC COUNTING CIRCUITS
Inverting and non-inverting gates in a variety of logic systems are discussed and a wide range of bistable (flip-flop) circuits including R-S, T, D and J-K are considered. Executions using discrete components and integrated circuits are described.

Chapter 4—PULSE SHAPING CIRCUITS
A pulse squaring circuit and a Schmitt trigger regenerative pulse shaping circuit are analysed. A monostable pulse forming circuit is examined.

Chapter 5—BINARY COUNTERS
Up, down and reversible forms of the most basic of counters (the binary counter) are described, using synchronous and asynchronous techniques.

Chapter 6—RING COUNTERS
Several one-out-of-ten ring counters with and without visual display are described. Use of a wide range of components including gasfilled trigger and display tubes, thyristors, silicon controlled switches, transistors and integrated bistable circuits is discussed.

Chapter 7—BINARY CODED DECIMAL COUNTERS
Counters using various binary-decimal codes are presented. Ripple-through and synchronous versions of up, down and reversible symmetrical and asymmetrical BCD counters using discrete components or integrated circuits are described.

Chapter 8—COUNTERS USING LESS COMMON CODES
Twisted-ring, Gray-code and one-out-of-five-flop counters are three of the examples that illustrate the use of less common counting codes.

Chapter 9—STORAGE
Bistable stages designed for storing a count are described. Neon tubes, cold cathode trigger tubes, silicon controlled switches and transistors are the storage elements considered.

Chapter 10—DECODING AND CODE CONVERSION
Conversion from various weighted and unweighted binary coded decimal counting codes into a decimal read-out is discussed in full. Simplification of the decoding circuits by combining redundant states using Veitch diagrams is illustrated.

Chapter 11—NUMERICAL INDICATOR TUBES
The construction, operation and application of devices —numerical indicator tubes—suitable for producing a visual display of the state of a counter are given.

Copies of the Mullard Counting Book can be obtained, price (U.K. only) 27s 6d plus 1s 6d postage and packing, from Distributor Sales Division, Mullard Limited, or from any of the usual Mullard Industrial Distributors.